

Self-synchronizing Series-connected Inverters

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Abstract—This paper describes a virtual oscillator based approach to synchronize series-connected single-phase inverters. Each inverter controller includes a digital implementation of a Van der Pol oscillator. When connected in series, such inverters synchronize automatically, without the need for a central controller, communication channels, phase locked loops, or additional hardware such as powerline communication. A linearization-based analysis is used to prove system stability of the synchronized state. The approach is experimentally verified on a 180 W system consisting of three 60 W inverters.

I. INTRODUCTION

In this paper, we examine the series-connected architecture of inverters serving a common resistive load shown in Fig. 1. Such an architecture has several advantages including: modularity, scalability, use of low-voltage devices, and the absence of high-step-up dc-dc conversion stages. As a result, it is suitable for dc-to-ac conversion in applications such as photovoltaic (PV) energy conversion systems, and energy storage systems.

Challenges in such a system are related to control techniques necessary to achieve low current distortion, power sharing, and synchronization among the modules at the line frequency, preferably without the need for a central controller or high-speed communication between the modules. Although several current-control and power-sharing techniques have been proposed for cascaded inverter systems [1]–[8], most existing methods require at least one centralized controller to synchronize the inverters (typically based on sensing the output voltage) and using a phase locked loop (PLL) to generate and distribute a synchronization signal to all modules. This requires additional wiring or additional hardware such as powerline communication (PLC) [9]. Controlling series connected inverters using a central or master controller is discussed in [1]–[4]. Control strategies proposed in [5]–[8] eliminate the need for high-speed switching signal communications between the modules but still require a line frequency heart beat signal for operation. Fully decentralized control of ac-stacked inverters is proposed in [9], but it requires installing additional hardware to enable PLC communication.

In this paper, we utilize a closed-loop inverter controller based on the Van der Pol (VDP) oscillator [10] to achieve communication-free synchronization among cascaded inverters. The control architecture is shown in Fig. 2. Indeed, with a communication-free controller, one obtains a truly autonomous and modular system. VDP oscillators have found applications

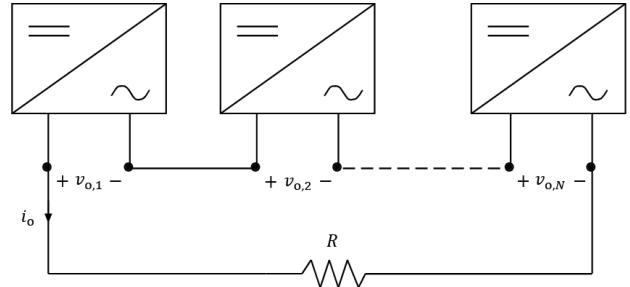


Figure 1: A system of N series connected inverters supplying a resistive load. Our approach guarantees synchronization of inverter outputs without communication.

in communication systems as frequency synthesizers and for frequency modulation. Coupled VDP oscillators have also been investigated in [11]–[13]. Coupled VDP oscillators in the context of power processing for parallel connected inverters has been explored in [14]–[16]. In this paper, we explore the application of VDP oscillators for series-connected inverters. These oscillators synchronize seamlessly and without communication when coupled through the system with the only communication provided by the intrinsically shared output current that is common to all inverters in the setup. As such, this work builds on prior results in [14], [17], which were limited to parallel connected inverters.

The remainder of this paper is structured as follows: Section II details the system dynamical model. Section III provides an averaged dynamical model of the system and provides a stability result pertaining to the synchronized state. Experimental results are provided in Section IV. Section V concludes the paper and details a few directions for future research.

II. DYNAMICAL SYSTEM MODEL

Each module in the series stack consists of the power stage and a controller as shown in Fig. 2. We discuss pertinent modeling details of each next.

A. Power stage

The power stage consists of a full-bridge inverter with a dc voltage source, V_{dc} , as the input (modeling, e.g., a PV panel or a battery). The differential switch-node voltage of the j -th inverter is denoted by $v_{sw,j}$. This voltage, averaged over

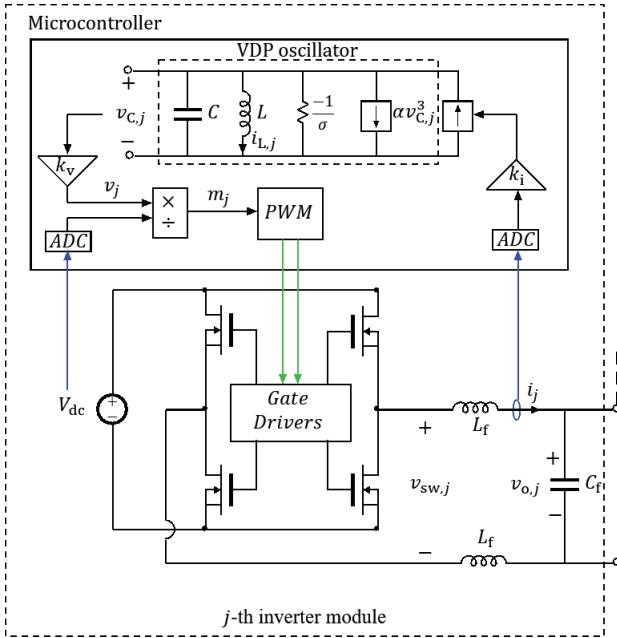


Figure 2: Inverter module showing the power stage and the controller. Note that the VDP oscillator based controller is implemented in the microcontroller locally, and only requires sensing of inductor current and input voltage which are also measured locally. This makes the system truly autonomous.

a switching period T_{sw} is termed the terminal voltage. It is denoted by v_j , and obtained as:

$$v_j(t) = \frac{1}{T_{\text{sw}}} \int_{s=t-T_{\text{sw}}}^t v_{\text{sw},j}(s) ds. \quad (1)$$

The modulation index m_j for PWM that governs this voltage is given by:

$$m_j(t) = \frac{v_j(t)}{V_{\text{dc}}}. \quad (2)$$

The full bridge is followed by an output filter (with inductance L_f and capacitance C_f). We use i_j and $v_{o,j}$ to denote the inductor current and the capacitor voltage of the j -th inverter filter respectively.

B. Controller Dynamics

The controller performs the following functions: i) sensing the dc input voltage V_{dc} and the inductor current i_j , ii) relaying the gate signals to control the full-bridge inverter; and iii) executing the dynamics of the discretized Van der Pol oscillator. We now describe the oscillator dynamics in detail.

The Van der Pol oscillator consists of inductance L and capacitance C which determine the resonant frequency $\omega = 1/\sqrt{LC}$ and quality factor $\varepsilon = \sqrt{L/C}$ of the oscillator. The virtual capacitor voltage of the j -th oscillator is denoted by $v_{C,j}$ and the inductor current is denoted by $i_{L,j}$. The non-conservative, non-linear damping nature of the oscillator comes from the negative conductance element $-\sigma$ along with the cubic voltage-dependent current source $\alpha v_{C,j}^3$, where α is a positive constant. Note that when $\alpha = 0$ and $\sigma = 0$, the Van der Pol oscillator reduces to a simple harmonic oscillator.

Since all the inverters are connected in series, they all have the same series current. Hence, current becomes a natural choice for coupling the oscillators as well. To this end, the filter inductor current, i_j , is used as the forcing term for the oscillators using a current coupling factor k_i . The virtual capacitor voltage $v_{C,j}$ is coupled back to the power stage using the voltage coupling factor k_v . The dynamics of the j -th inverter controller can then be described using the following differential equations:

$$L \frac{di_{L,j}}{dt} = v_{C,j} = \frac{v_j}{k_v}, \quad (3)$$

$$C \frac{dv_{C,j}}{dt} = -\alpha \frac{v_{C,j}^3}{k_v^3} + \sigma k_v v_{C,j} - k_v i_{L,j} + k_v k_i i_j. \quad (4)$$

The oscillator dynamics are discretized for digital implementation in the microcontroller. Such discretization techniques have been previously discussed in [14], [18], [19].

III. STABILITY ANALYSIS

In this section, we first build a model for the coupled system and then present a stability result for synchronization of the inverter output voltages. By the way of notation, N inverters are indexed by the set $\mathcal{N} := \{1, \dots, N\}$. For the purpose of analysis in this section, recall that ε, k_v, k_i are all positive scalars; their signs are instrumental in deciding the nature of the stable solutions.

A. Averaged Model

As laid down in the previous section, the dynamics of the j -th oscillator can be written as:

$$\begin{aligned} \dot{x}_j &= \frac{dx}{dt} = \omega y_j, \\ \dot{y}_j &= \frac{dy}{dt} = -\omega x_j + \varepsilon \omega \sigma g(y_j) + \varepsilon \omega k_v k_i i_j, \end{aligned} \quad (5)$$

where $x_j = k_v \varepsilon i_{L,j}$, $y_j = v_j$ and $g(y_j) = y_j - \frac{\alpha}{k_v^2 \sigma} y_j^3$.

The analysis in this section is for line frequency dynamics. To this end, the filter inductor current averaged over a switching period is approximately equal to the system output current, i_o .

$$\frac{1}{T_{\text{sw}}} \int_{s=t-T_{\text{sw}}}^t i_j(s) ds \approx i_o. \quad (6)$$

Similarly, the differential switch node voltage averaged over a switching period is approximately equal to the output voltage.

$$v_j \approx v_{o,j}. \quad (7)$$

We can then write the coupling introduced by the virtue of the electrical interconnection through current i_o as:

$$i_o = \frac{k_v}{R} \sum_{j=1}^N y_j, \quad (8)$$

where R is the load resistor connected to the series stack. To derive the phase dynamics, we convert the model in (5) to polar coordinates using the coordinate transformation $x_j := V_j \sin(\omega t + \theta_j)$ and $y_j := V_j \cos(\omega t + \theta_j)$ and leveraging

the method of periodic averaging to obtain an approximate time-invariant description that is $\mathcal{O}(\varepsilon)$ close to the original dynamics [20] and easier to analyze. The averaged-system dynamics are given by:

$$\begin{aligned}\dot{\bar{V}}_j &= \varepsilon \bar{g}(\bar{V}_j) + \frac{\varepsilon k_v k_i}{2R} \sum_{k=1}^N \bar{V}_k \cos \bar{\theta}_{jk}, \\ \dot{\bar{\theta}}_j &= -\frac{\varepsilon k_v k_i}{2R \bar{V}_j} \sum_{k=1}^N \bar{V}_k \sin \bar{\theta}_{jk}.\end{aligned}\quad (9)$$

B. Local Exponential Stability of Synchronized Trajectories

In this section, leveraging the averaged dynamical model in (9), we establish the local stability of the synchronized solutions by looking at the linearization; this result is provided next.

Theorem 1. *The synchronized solutions, i.e., $\bar{V}_j(t) = \bar{V}_k(t), \bar{\theta}_{jk} = 0 \forall j, k \in \mathcal{N}$ are locally exponentially stable for the coupled system dynamics described by (9).*

Proof. The Jacobian J in this case has a upper block diagonal structure:

$$J := \begin{bmatrix} \bar{g}'(\rho) I_N & J' \\ 0 & -\frac{\varepsilon k_v k_i}{2R} L \end{bmatrix}, \quad (10)$$

where I_N is the $N \times N$ identity matrix and $\rho > 0$ is the unique positive solution which satisfies $\bar{g}(\rho) = 0$. Recall that $\bar{g}(.)$ is a cubic function with identical coefficients for all the inverters and we denote L to be the Laplacian matrix of the underlying undirected fully-connected graph. Since we know that $\bar{g}'(\rho) < 0$, so $\bar{g}'(\rho) I_N$ has negative eigenvalues. Furthermore, we know L is positive semi-definite for a simple connected graph [21], and has 1_N (length- N vector with all entries equal to one) as eigenvector in its nullspace (associated with the simple 0 eigenvalue) which is orthogonal to the space spanned by eigenvectors with positive eigenvalues. Notice that by traversing the 1_N direction, the system still remains synchronized, i.e., if the phases of all the inverters change by exact same amount, they are still synchronized. Consequently, $-\frac{\varepsilon k_v k_i}{2R} L$, where $\frac{\varepsilon k_v k_i}{2R} > 0$, has exactly the same properties only with the sign of the eigenvalues flipped. Hence, the synchronized solutions are locally exponentially stable. ■

IV. EXPERIMENTAL RESULTS

To validate the theory, experiments were conducted on a system with a power rating of 180 W and three 60 W inverters connected in series. A single inverter module is shown in Fig. 3. The Delfino control card TMS320F28379D from Texas Instruments was used to implement the discretized oscillator-based controllers.

A. System Design

The analysis in this section assumes equal power sharing among the modules, i.e., the synchronized steady-state RMS

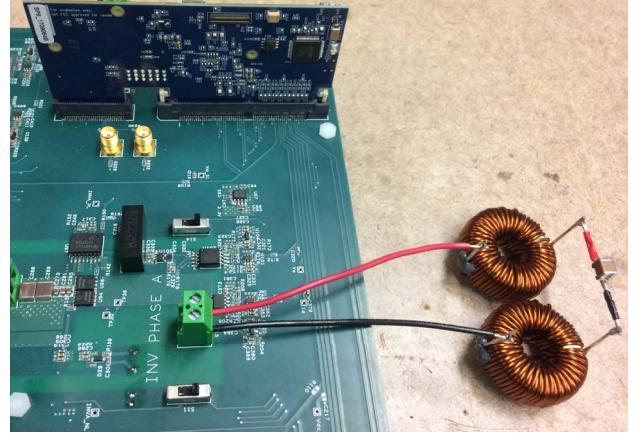


Figure 3: Hardware prototype of a single 60 W inverter module showing the power stage and the controller.

terminal voltage, $V_{ss,j}$ is the same across all the modules and denoted to be V_{eq} :

$$V_{ss,1} = V_{ss,2} = \dots = V_{ss,N} = V_{eq}. \quad (11)$$

For a given system load, P_{sys} , we can follow the analysis laid out in [14] for islanded inverter design and apply the techniques for the case of series connected inverters. We then obtain the following equation for the steady state RMS voltage of the inverters as a function of the system power:

$$V_{eq} = k_v \left(\frac{\sigma + \sqrt{\sigma^2 + 6\alpha(k_i/k_v)(P_{sys}/N)}}{3\alpha} \right). \quad (12)$$

Note that the steady-state voltage is dependent on: i) oscillator parameters σ and α , ii) coupling parameters k_i and k_v , and, iii) system parameters N and P_{sys} . A procedure to select these parameters is given next.

Consider a system of N inverter modules connected in series with a power rating of P_{rated} . It is desired to keep the output voltage of each inverter module within V_{oc} (steady-state open-circuit RMS voltage) and V_{max} (maximum acceptable steady-state RMS voltage) as the system power varies from no load to the rated power. This voltage regulation criteria helps us pick the values for the coupling coefficients k_v , k_i and also the oscillator parameters σ and α :

$$k_v = V_{oc}, \quad k_i = \frac{V_{max}N}{P_{rated}}, \quad (13)$$

$$\sigma = \frac{V_{oc}}{V_{max}} \frac{V_{oc}^2}{V_{max}^2 - V_{oc}^2}, \quad \alpha = \frac{2\sigma}{3}. \quad (14)$$

The L and C values of the oscillator can be chosen depending on the desired rise time, t_{rise} , acceptable ratio of third harmonic to the first harmonic, $\delta_{3:1}$ and the required line frequency of operation:

$$C = \frac{\sigma}{4} \left(\frac{t_{rise}}{3} + \frac{1}{4\omega\delta_{3:1}} \right), \quad L = \frac{1}{C\omega^2}. \quad (15)$$

The circuit parameters of each inverter are given in Table I. The system specifications are provided in Table II while

Table I: Circuit Parameters

V_{dc}	Input voltage of each module	25 V
C_f	Filter capacitor	$22 \mu\text{F}$
L_f	Filter inductor	$470 \mu\text{H}$
f_{sw}	Switching frequency	10 kHz

Table II: System Specifications

V_{oc}	Open-circuit voltage per module	12 V (RMS)
P_{rated}	System rated power	180 W
V_{max}	Voltage at rated power per module	15 V (RMS)
ω	Nominal system frequency	$2\pi 50 \text{ rad/s}$
t_{rise}	Rise time	2 s
$\delta_{3:1}$	Ratio of third-to-first harmonic	2 %

the control parameters that achieve these specifications are calculated using equations (13) through (15) and are listed in Table III.

B. Experiment: Equal power sharing

Experimental results for equal power sharing among the series-connected inverters with different loads of 50 W, 90 W, and 160 W are shown in Fig. 4, Fig. 5, and Fig. 6, respectively. During the system turn ON, the capacitor voltages and inductor currents in each of the VDP oscillators are non-identical. As a result, the output voltages of the inverters are not in sync. The series output current of the system couples the oscillators and eventually, the output voltages of the inverters synchronize, building up the voltage across the series stack.

Table III: Controller Parameters

k_v	Voltage-scaling factor	12 V/V
k_i	Current-scaling factor	0.25 A/A
σ	Conductance	$1.42 \Omega^{-1}$
α	Coefficient of cubic current source	0.95 A/V^3
C	VDP-oscillator capacitance	0.25 F
L	VDP-oscillator inductance	$40.5 \mu\text{H}$

C. Experiment: Unequal power sharing

The coupled VDP oscillators synchronize even when individual inverters in the series stack process unequal power. To accommodate unequal power sharing between the inverter modules, the value of the voltage coupling factor, k_v , can be adjusted. This can be achieved using a battery management controller in case of an energy storage system or a maximum power point tracker (MPPT) in case of a photovoltaic system. Experimental results for unequal power sharing are given in Fig. 7 where the three modules share 39%, 33% and 28% of the system power. This is evident from the steady-state output voltage waveforms of the three inverters.

D. Performance evaluation

The load characteristics of the 180 W system can be plotted using (12) and is shown in Fig. 8. It is clear from (12) that the steady state voltage of the inverter modules increases as the system power increases, but it is kept within the regulation limits as specified by the system requirements. Experimental results match the theoretically predicted values.

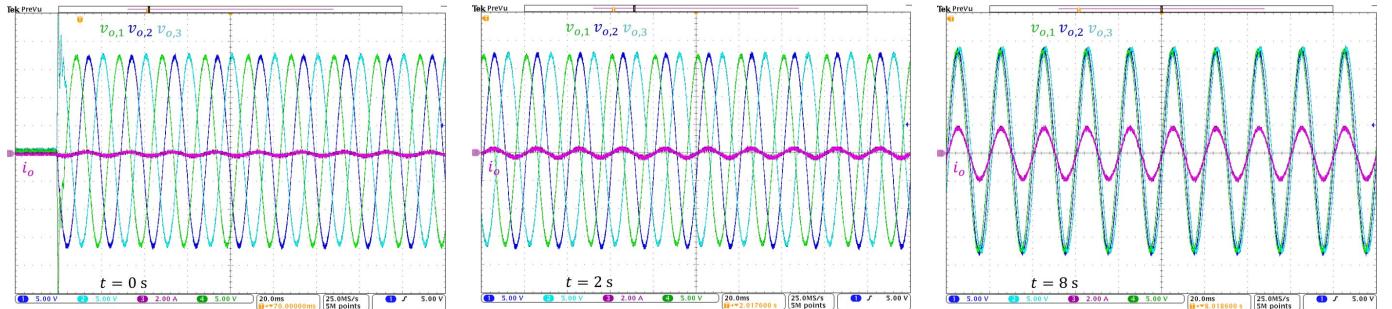


Figure 4: Experimental waveforms showing the start-up transient with a 50 W load. The steady-state RMS voltage of all the inverters are the same and are equal to 12.8 V, while the steady-state series RMS current is 1.3 A.

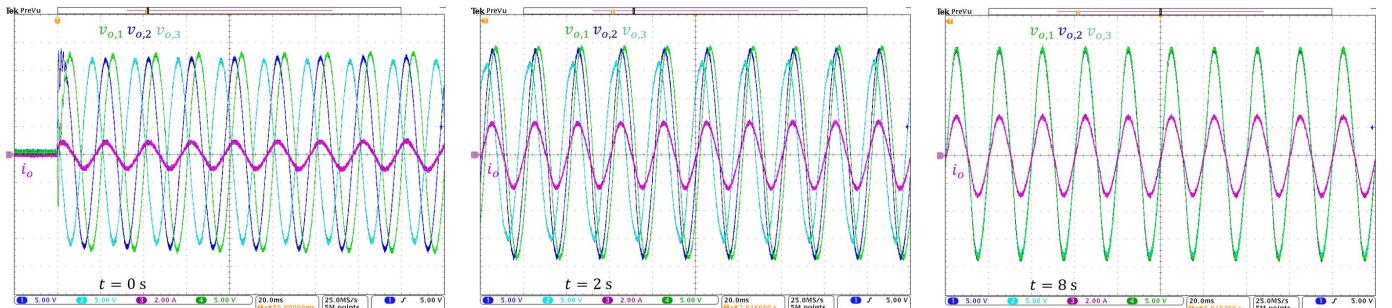


Figure 5: Experimental waveforms showing the start-up transient with a 90 W load. The steady-state RMS voltage of all the inverters are the same and are equal to 13.7 V, while the steady-state series RMS current is 2.2 A.

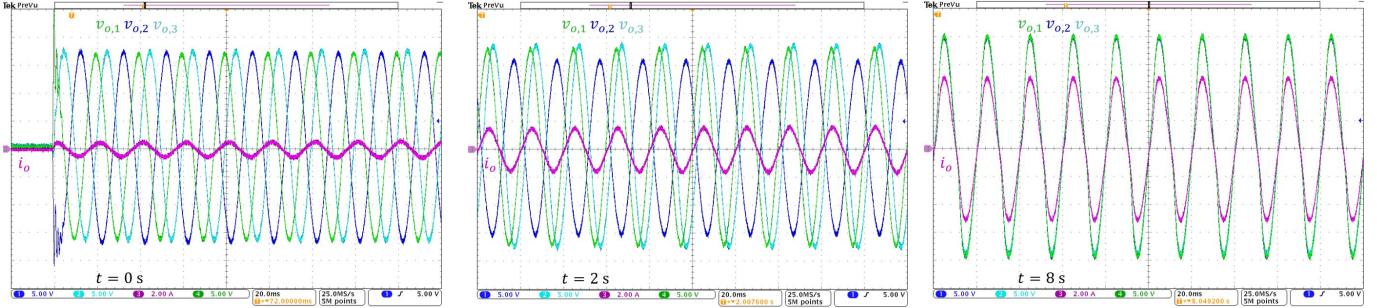


Figure 6: Experimental waveforms showing the start-up transient with a 160 W load. The steady-state RMS voltage of all the inverters are the same and are equal to 14.4 V, while the steady-state series RMS current is 3.7 A.

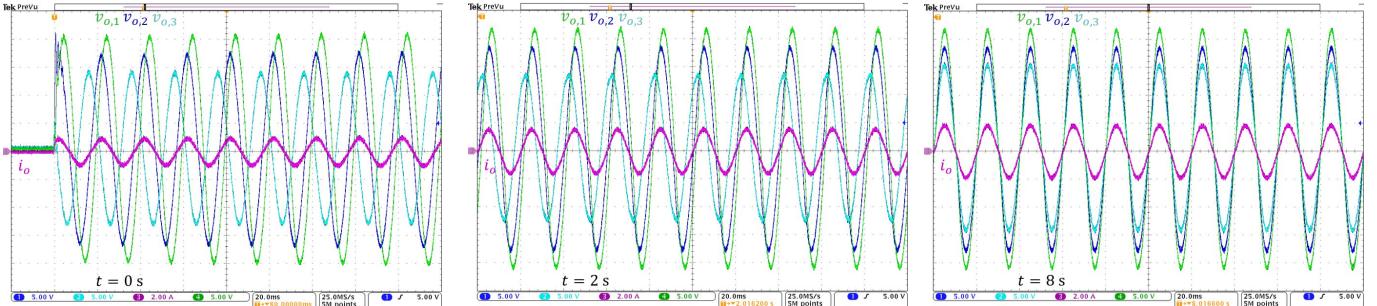


Figure 7: Experimental waveforms showing the start-up transient with a 50 W load with unequal power sharing among the modules. The steady-state RMS voltages of the inverters are 15.5 V, 13.4 V and 11.3 V while the steady-state series RMS current is 1.3 A.

To evaluate the dynamic performance of this synchronization process, we define synchronization error $e[k]$, over a moving window of length $2\pi/\omega$ as:

$$e[k] = 1 - \frac{1}{N\sqrt{2}V_{eq}} \max \left(\sum_{j=1}^N v_{o,j}(t) \Big|_{t=k2\pi/\omega}^{(k+1)2\pi/\omega} \right), \quad (16)$$

where $k \in \mathbb{Z}$. The continuous-time version of the synchronization error can then be constructed using a weighted dirac-delta functions as follows:

$$e(t) = \sum_{k=-\infty}^{\infty} e[k] \delta \left(\frac{t - k2\pi/\omega}{2\pi/\omega} \right). \quad (17)$$

This error is plotted using the data from the experimental results corresponding to $N=3$ for various load powers with equal power sharing and is shown in Fig. 9.

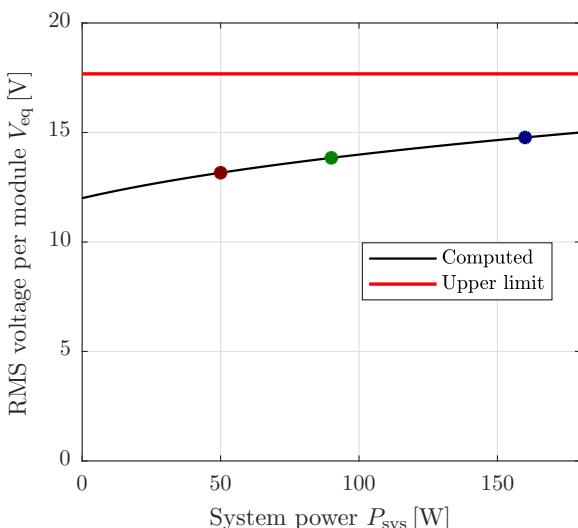


Figure 8: Load characteristics of the series stacked system. As the system power varies from no load to the full rated power, the RMS voltage per module increases. The dots on the curve depict the experimentally verified values.

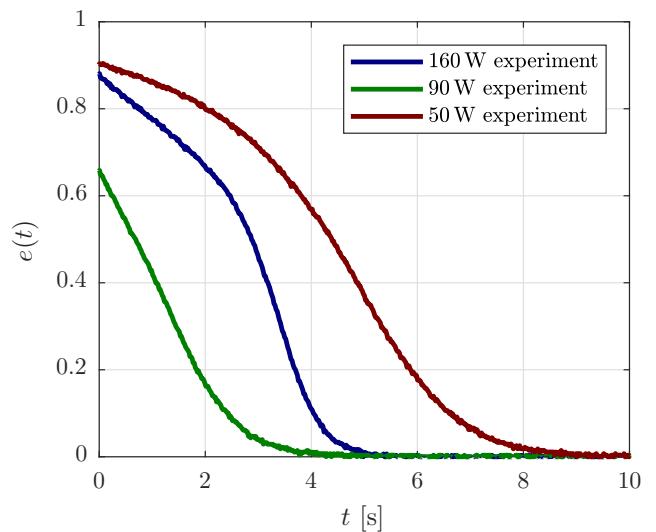


Figure 9: Synchronization error.

V. CONCLUSIONS

This paper presented the design and implementation of a communication-free modular control structure for series-connected inverters. This is made possible by the use of discretized Van der Pol oscillators serving as the controllers. The inverter modules are coupled to the oscillators using the series current in the system. A model for the coupled system is presented and a proof for local exponential stability is also provided. System operation is experimentally verified on a 180 W system with three inverters connected in series. The proposed system eliminates the need for a global PLL, additional wiring for communication or additional hardware such as powerline communication. These features make this system truly autonomous and highly advantageous for scalable and modular applications. Future work will explore reactive power handling and grid connected system architectures.

ACKNOWLEDGEMENTS

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