

Minimum Distortion Point Tracking: Optimal Phase Shifting for Input- or Output-Parallel Connected DC-DC Converters

Jason Poon*, Brian B. Johnson†, Sairaj V. Dhople‡, Seth R. Sanders*

*EECS Department, University of California, Berkeley
email: {jason, seth.sanders}@berkeley.edu

†EE Department, University of Washington, Seattle
email: brianbj@uw.edu

‡ECE Department, University of Minnesota
email: sdhople@umn.edu

Abstract—This paper introduces the notion of *minimum distortion point tracking (MDPT)*: a control paradigm for input- or output-parallel connected dc-dc converters where switching waveforms are optimally phase shifted to minimize the total dc-bus ripple power. In a sense, MDPT generalizes the ubiquitous concept of interleaving in balanced multiphase dc-dc converters to a broad class of asymmetric input- or output-parallel connected dc-dc converters. Realizing power-quality improvement with control design implies that a drastic reduction in passive input or output filters can be achieved. This paper presents the mathematical characterization of the minimum distortion point (MDP) and a technique for MDPT. An experimental case study for three 600 W dc-dc converters demonstrates a $3\times$ reduction in the bus voltage ripple, convergence to a static MDP in 40 ms, and the ability to dynamically track a time-varying MDP.

I. INTRODUCTION

Input- or output-parallel connected dc-dc converters are ubiquitous in many power electronics systems, such as point-of-load conversion systems, dc microgrids, and integrated circuits with multiple on-die voltage domains. While it is well recognized that symmetric phase shifting (i.e., interleaving) minimizes ripple power in balanced multiphase dc-dc converters [1], [2], the optimal strategy for phasing shifting a collection of input- or output-parallel connected dc-dc converters with asymmetries or non-uniform operation has largely been unaddressed. Such asymmetries may arise from independent source or load connections (as in point-of-load conversion systems) or from non-idealities in converter passive or active components (as is common in VRMs). Existing literature has focused on first harmonic elimination techniques [3] and randomized modulation schemes [4], [5], among others.

This paper introduces a new control paradigm, termed *minimum distortion point tracking (MDPT)*, which generalizes the notion of interleaving in balanced multiphase dc-dc converters to a broad class of asymmetric input- or output-parallel connected dc-dc converters. We present the concept of the *minimum distortion point (MDP)*, which establishes a first principles limit on the minimum ac ripple power for a network of input- or output-parallel connected dc-dc converters. In particular, the MDP is defined as the phase shift across the converters that minimizes the ac power of the dc-bus capacitor voltage. Minimization of this ac power is desirable in that it is precisely this quantity that determines the minimum filtering needed to satisfy a maximum ripple or harmonic frequency content constraint on the bus voltage or current. Using this definition, we present and experimentally demonstrate practical techniques for achieving MDPT, i.e., online methods of identifying and perturbing the system towards the MDP. The experimental case study considered here demonstrates a $3.01\times$ reduction in the bus voltage ripple for a static MDP with convergence occurring in 40 ms. Moreover, we demonstrate the ability to dynamically track a time-varying MDP over a wide operating range.

Compared to existing literature, the proposed minimum distortion point tracking distinguishes itself in its: i) *generality*—the theory, analyses, and techniques can be applied to any asymmetric input- or output-parallel connected dc-dc converter regardless of whether the asymmetry arises from the topology or the operating condition, and ii) *optimality*—it establishes a first principles limit on the minimum ac ripple power that is attainable with phase shifting.

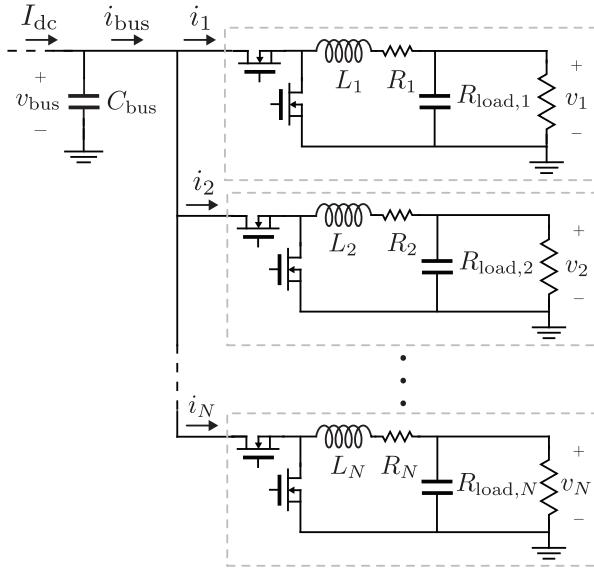


Fig. 1: N input-parallel connected dc-dc buck converters with independent output voltages v_1, \dots, v_N and load resistances $R_{\text{load},1}, \dots, R_{\text{load},N}$.

The remainder of this paper is organized as follows. Section II presents the mathematical principles and numerical analyses to describe the *minimum distortion point* (MDP). Section III presents a gradient-descent-based technique for *minimum distortion point tracking* (MDPT). Section IV presents experimental validation of the proposed concepts on a prototype consisting of three input-parallel connected 600 W dc-dc converters. Section V concludes the paper.

II. CHARACTERIZING THE MINIMUM DISTORTION POINT (MDP)

In this section, we define the *minimum distortion point* (MDP) in a precise mathematical sense. The following developments consider a system of N dc-dc buck converters operating at periodic steady state with identical switching frequencies, f_s , and connected in parallel at the input (see Fig. 1). The analysis, however, can be generalized to: i) different converter systems (e.g., converters connected in parallel at the output) or ii) different dc-dc converter topologies. Following this mathematical definition, we will demonstrate typical performance enhancements that are achievable when operating at the MDP and compare operation with symmetric interleaving through a numerical simulation.

A. Mathematical Principles of the MDP

For a system of N dc-dc converters, collect the relative phase spacings between converters in the length $\binom{N-1}{2}$ vector $\theta := [\theta_{21}, \theta_{32}, \dots, \theta_{N(N-1)}]^T$, with θ_{jk} denoting the phase spacing between the switching waveforms of the j and k converter, respectively. Furthermore, denote

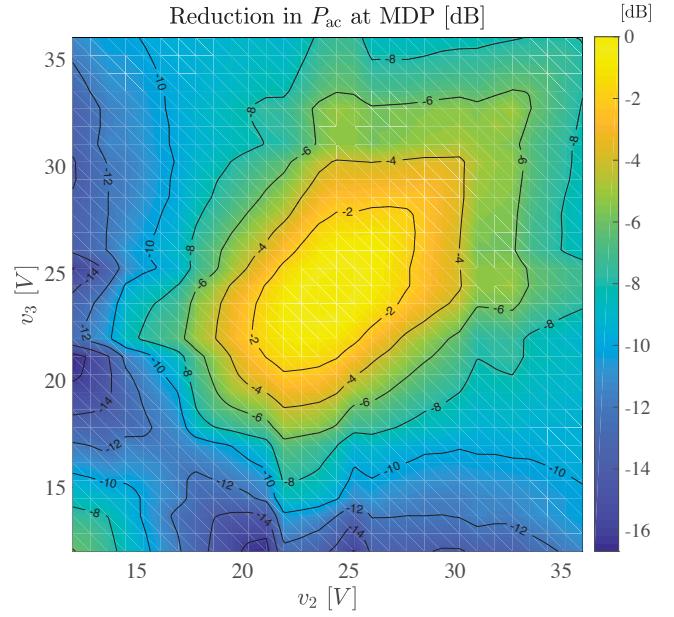


Fig. 2: Reduction in P_{ac} between the symmetric interleaved state and the MDP when $v_1 = 24$ V.

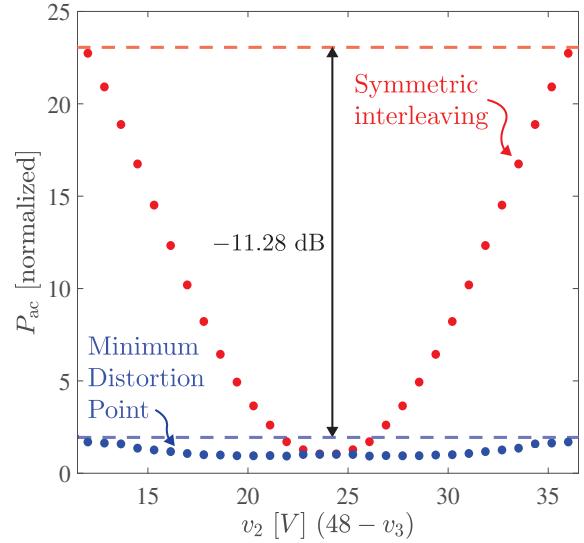


Fig. 3: Reduction in P_{ac} between the symmetric interleaved state and the MDP when $v_1 = 24$ V and $v_3 = 48 - v_2$.

v_{bus} as the ac voltage across C_{bus} , and P_{ac} as the ac (ripple) power corresponding to this voltage. The MDP is characterized by the θ that—in principle—globally minimizes an unconstrained optimization problem whose cost function is the quantity P_{ac} . Precisely, the MDP corresponds to converter operation with the following phase spacing:

$$\theta^* = \arg \min_{\theta} P_{\text{ac}}. \quad (1)$$

The explicit parametric dependence of P_{ac} on θ can be obtained by calculating the L_2 -norm of the Fourier coefficients corresponding to v_{bus} . For the particular

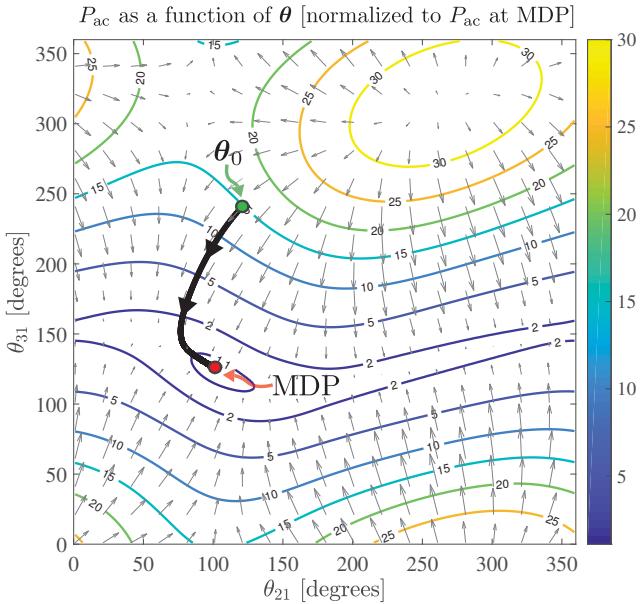


Fig. 4: Numerical simulation of the proposed gradient descent-based MDPT technique. Contour lines of P_{ac} (normalized to P_{ac} at the MDP) and arrows depicting ∇P_{ac} are shown.

example of the input-parallel connected buck converters illustrated in Fig. 1, these coefficients can be obtained by computing the Fourier series of each input current, i_ℓ , $\forall \ell = 1, \dots, N$, taking the sum of these series to obtain the corresponding series for i_{bus} and then scaling by the capacitive impedance $1/(j\omega C_{bus})$. It so emerges that the closed-form analytical expression for P_{ac} is:

$$P_{ac} = \sum_{k=1}^K \sum_{n=1}^N (\beta_n^k)^2 + 4 \sum_{k=1}^K \sum_{j=1}^N \sum_{i=1}^{j-1} \beta_i^k \beta_j^k \cos(\theta_{ij}), \quad (2)$$

where β_ℓ^k is a scaled version of the k -th Fourier-series coefficient of i_ℓ , α_ℓ^k . The precise definitions of α_ℓ^k and β_ℓ^k as well as the complete derivation of the above expression are given in the Appendix.

B. Analysis of the MDP with a Numerical Example

We will now analyze system performance at the MDP using a numerical simulation. In particular, we will attempt to quantify the achievable performance enhancement compared to operation at the symmetric interleaved state.

Consider the topology in Fig. 1 for the particular case of $N = 3$ converters, and with component parameters and operating conditions indicated in Table I. Note that we will operate this system to induce asymmetry (so as to compare results with symmetric interleaving) with different output voltages, v_1, v_2 , and v_3 , since the component parameters in each phase are otherwise identical. We perform two different operating sweeps on this system. First, we fix $v_1 = 24$ V and sweep both

v_2 and v_3 independently from 12 V to 36 V. We record the reduction in P_{ac} between the symmetric interleaved state and the MDP. The results of this sweep are shown in Fig. 2. A few interesting points can be noted from this result: i) at certain operating points, the reduction in P_{ac} exceeds 16 dB; ii) P_{ac} is lower at the MDP across every operating point in this sweep; and iii) at the point of symmetry, $v_1 = v_2 = v_3 = 24$ V, symmetric interleaving indeed provides the optimal P_{ac} and is equivalent to the MDP.

Next, we perform a sweep in which v_1 is held constant at 24 V while v_2 and v_3 are swept such that $v_3 = 48 - v_2$. The results of this sweep are shown in Fig. 3, where P_{ac} is normalized to the P_{ac} obtained when $v_1 = v_2 = v_3 = 24$ V (at this point, P_{ac} at the symmetric interleaved state and the MDP are identical). Across this sweep range, we note that the worst case P_{ac} at the MDP is -11.28 dB ($13.4\times$) lower than the worst case P_{ac} at the symmetric interleaved state. One practical implication of this result is that the capacitance requirement for C_{bus} to achieve the same output voltage ripple in v_{bus} is reduced by a factor of $3.6\times$.

III. TECHNIQUE FOR MINIMUM DISTORTION POINT TRACKING (MDPT)

With the MDP formally introduced and characterized, we now present a method for *minimum distortion point tracking* (MDPT). In this paper, we focus on the gradient descent method [6]. The gradient descent-based MDPT uses the gradient of P_{ac} to determine a direction and magnitude in which to perturb θ . By perturbing θ iteratively using this technique, the system converges to the operating point that (locally) minimizes P_{ac} . In particular, we adopt the following update rule for the $q+1$ update of θ :

$$\theta[q+1] = \theta[q] - \kappa \nabla P_{ac}(\theta[q]) \quad (3)$$

where $\nabla P_{ac}(\theta[q])$ is the gradient of P_{ac} with respect to θ at the q update instant, and κ is a scalar that can be empirically determined to trade off between numerical stability and convergence speed. Note that since P_{ac} is not necessarily a convex function of θ , the gradient descent-based MDPT may track local minima depending on the initial condition. In practice, numerical simulations can be used to verify: i) if multiple minima exist, and ii) what performance variations could manifest depending on which minima the system converges to.

Next, we will perform a numerical simulation to verify the operation of the proposed gradient descent-based MDPT. Again, consider the topology in Fig. 1 for $N = 3$ and with the component parameters and operating conditions as indicated in Table I. We consider a static

TABLE I: Parameters and components for numerical simulations and experimental prototype.

Parameters/Component	Value
v_{bus}	48 V
C_{bus}	300 μ F
L_ϕ	141.6 μ H
R_ϕ	13.7 m Ω
Switching frequency	20 kHz
Control device	Xilinx Artix-7 XC7A35T

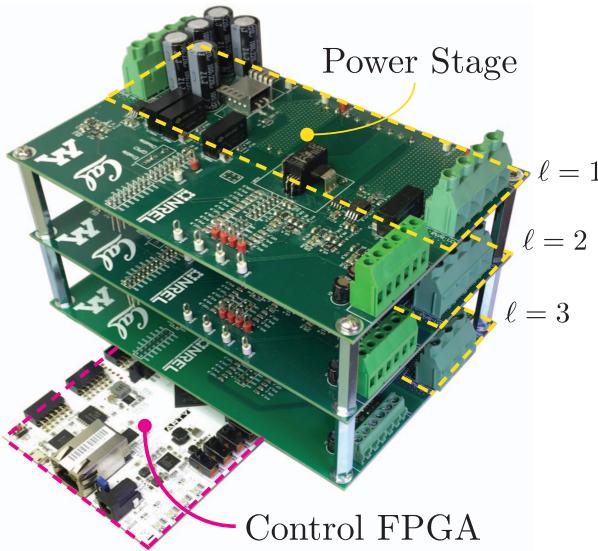


Fig. 5: Hardware prototype consisting of three 600 W input-parallel connected dc-dc buck converters with 48 Vdc input bus.

operating scenario in which $v_1 = 36$ V, $v_2 = 24$ V, and $v_3 = 12$ V.

The system is initialized at the symmetric interleaved state (i.e. $\theta_{21} = 120^\circ$ and $\theta_{31} = 240^\circ$). We use the gradient update function in (3) to perturb θ iteratively from the symmetric interleaved initial condition. Figure 4 shows the results of the numerical simulation: θ is perturbed orthogonally to the contour lines of P_{ac} and the algorithm converges to the MDP, in this case, at $\theta_{21} = 103^\circ$ and $\theta_{31} = 123^\circ$. For the particular system, P_{ac} is reduced by 11.6 dB (14.6 \times) at the MDP compared to operation at the symmetric interleaved state.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

In order to experimentally validate the MDPT concept, a hardware prototype consisting of three input-parallel connected dc-dc buck converters was constructed, as shown in Fig. 5. Table I presents the parameter and component values for this hardware prototype.

First, we validated the convergence speed and performance of the proposed MDPT algorithm. We introduced asymmetry in the resistive loads of each converter ($R_{load,1} = 2.4 \Omega$, $R_{load,2} = 1.2 \Omega$, and $R_{load,3} = 1.2 \Omega$) and also in the output voltages of each converter

($v_1 = 36$ V, $v_2 = 24$ V, and $v_3 = 12$ V). As shown in Fig. 6, the system is initialized at the symmetric interleaved state. The MDPT algorithm operates at an update rate of 2.5 kHz, eight times slower than the switching frequency of each converter. When the MDPT algorithm is initialized, the algorithm requires approximately 100 iterations (40 ms) to converge to the MDP. At this point, the voltage ripple in v_{bus} is reduced 3.01 \times compared to the voltage ripple at the symmetric interleaved state.

Second, we validated the tracking capability of the MDPT algorithm in scenarios when the converter operating condition (and thus, the MDP) is changing with respect to time. In this experiment, the resistive loads of each converter are identical ($R_{load,1} = R_{load,2} = R_{load,3} = 2.4 \Omega$), and the output voltages are initialized identically such that $v_1 = v_2 = v_3 = 24$ V. Then, v_2 is changed linearly from 24 to 36 V at a rate of 24 V/s, while v_3 is changed linearly from 24 to 12 V at the same rate. The voltage v_1 is held constant at 24 V.

As shown in Fig. 7(a), when symmetric interleaving is applied to this scenario, the voltage ripple in v_{bus} is minimized when the output voltages are identical, as expected. However, when the asymmetries in the output voltages are introduced, the voltage ripple increases monotonically, and reaches a maximum when $v_2 = 36$ V and $v_3 = 12$ V. At this point, the voltage ripple in v_{bus} is 3.28 \times larger than when the output voltages are identical.

When MDPT is applied to this scenario, as shown in Fig. 7(b), the voltage ripple in v_{bus} stays relatively constant, even as the asymmetries in the output voltages are introduced. At the point when $v_2 = 36$ V and $v_3 = 12$ V, the voltage ripple in v_{bus} is only 1.48 \times larger than when the output voltages are identical. This translates to a 2.20 \times improvement compared to the voltage ripple when symmetric interleaving is applied at this point. In this way, the MDPT approach is demonstrated to be effective at dynamically tracking the MDP and continuously minimizing the voltage ripple in v_{bus} over the given operating range.

V. CONCLUSIONS

We have shown that *minimum distortion point tracking* (MDPT) enables optimal minimization of ripple power in asymmetric input- or output-parallel connected dc-dc converters. To date, such problems have been largely only studied in balanced multiphase dc-dc converters with symmetric interleaving. In practice, MDPT has the potential to enable substantial enhancements in power density and efficiency by reducing the required filtering while maintaining or improving power quality for such converter systems.

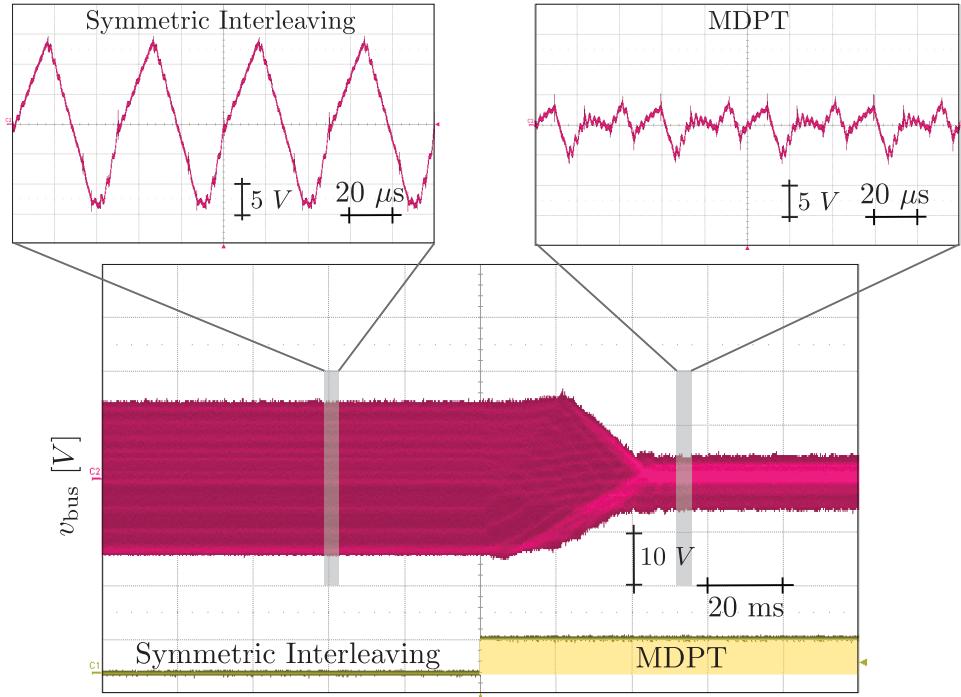


Fig. 6: Experimental validation of the convergence speed and performance of the proposed MDPT algorithm. As shown, the algorithm converges in approximately 100 iterations (40 ms) and enables a 3.01 \times reduction in the voltage ripple of v_{bus} compared to the voltage ripple at the symmetric interleaved state.

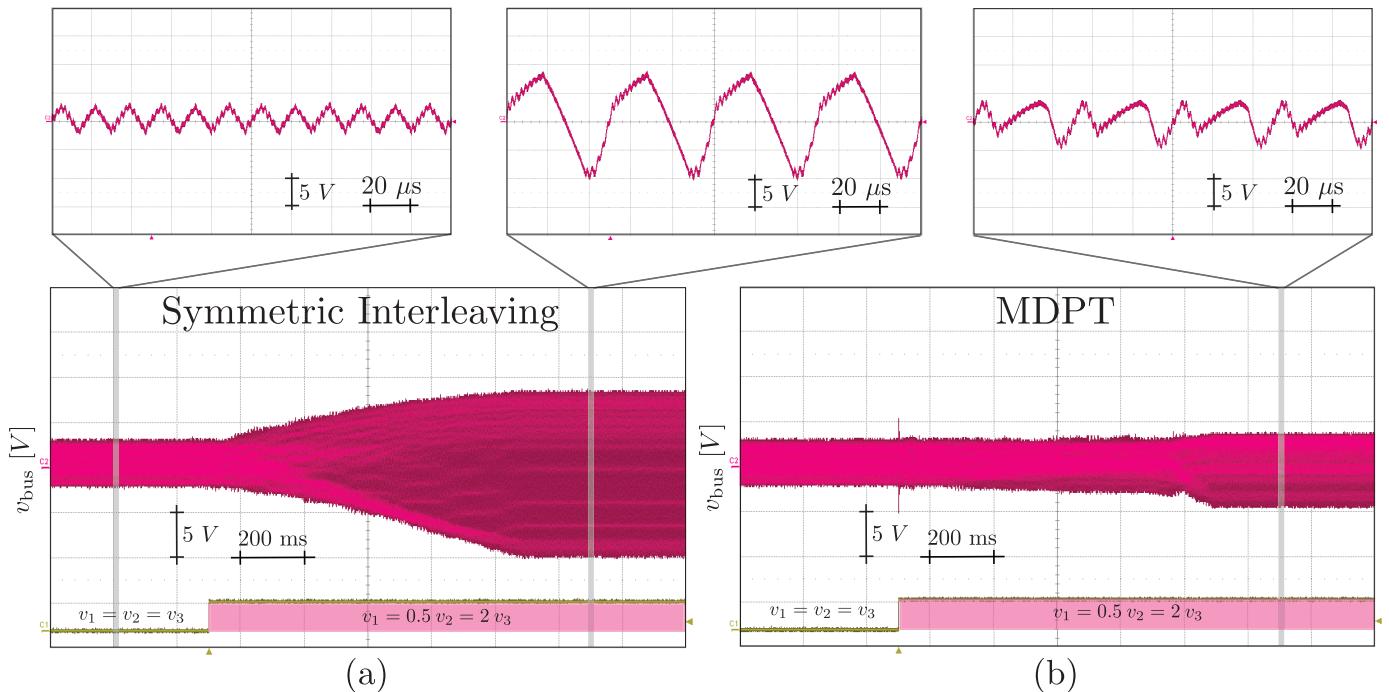


Fig. 7: Experimental validation of the tracking capability of the proposed MDPT algorithm. When asymmetries in the output voltages are introduced, (a) symmetric interleaving results in a 3.28 \times larger ripple in v_{bus} at the worst case, while (b) MDPT enables ripple minimization throughout the output voltage transient and results in only 1.48 \times larger ripple in v_{bus} at the worst case.

REFERENCES

- [1] C. Chang and M. A. Knights, "Interleaving technique in distributed power conversion systems," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, pp. 245–251, May 1995.
- [2] M. Sinha, S. Dhopole, B. Johnson, M. Rodriguez, and J. Poon, "Decentralized interleaving of paralleled dc-dc buck converters," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–6, July 2017.
- [3] M. Schuck and R. C. N. Pilawa-Podgurski, "Ripple minimization through harmonic elimination in asymmetric interleaved multi-phase dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 30, pp. 7202–7214, Dec 2015.
- [4] A. M. Stankovic, G. E. Verghese, and D. J. Perreault, "Analysis and synthesis of randomized modulation schemes for power converters," *IEEE Transactions on Power Electronics*, vol. 10, pp. 680–693, Nov 1995.
- [5] S. Banerjee and G. Verghese, *Nonlinear Phenomena in Power Electronics: Bifurcations, Chaos, Control, and Applications*. Wiley, 2001.
- [6] S. Boyd and L. Vandenberghe, *Convex Optimization*. New York, NY, USA: Cambridge University Press, 2004.
- [7] A. V. Oppenheim, A. S. Willsky, and S. H. Nawab, *Signals and Systems (2nd Ed.)*. Upper Saddle River, NJ, USA: Prentice-Hall, Inc., 1996.

APPENDIX

Uncovering the dependence of P_{ac} on θ

Consider the topology in Fig. 1. Let v_{bus} be the ripple (ac) voltage across C_{bus} . We assume that I_{dc} contributes the dc component of i_{bus} , while C_{bus} contributes the ac component of i_{bus} . In this way, v_{bus} is exclusively a function of the ac component of i_{bus} . The input current to each converter i_ℓ has a real-form Fourier series:

$$i_\ell(t) = \frac{a_\ell^0}{2} + \sum_{k=1}^{\infty} a_\ell^k \cos(2\pi kt) + b_\ell^k \sin(2\pi kt). \quad (4)$$

The Fourier coefficients a_ℓ^k and b_ℓ^k are given by:

$$a_\ell^k = \frac{2}{D_\ell \xi_k^2} \Delta I_\ell \cos(D_\ell \xi_k) + \frac{1}{\xi_k} (\Delta I_\ell + 2I_\ell) \sin(D_\ell \xi_k), \quad (5)$$

$$b_\ell^k = \frac{2}{D_\ell \xi_k^2} \Delta I_\ell \sin(D_\ell \xi_k) + \frac{1}{\xi_k} (\Delta I_\ell - 2I_\ell + (\Delta I_\ell + 2I_\ell) \cos(D_\ell \xi_k)), \quad (6)$$

where $\xi_k = 2\pi kT$ and ΔI_ℓ , I_ℓ , D_ℓ , and T are pictorially defined in Fig. 8. We can express (4) in complex-exponential form as:

$$i_\ell(t) = \sum_{k=-\infty}^{\infty} \alpha_\ell^k e^{j2\pi kt}, \quad (7)$$

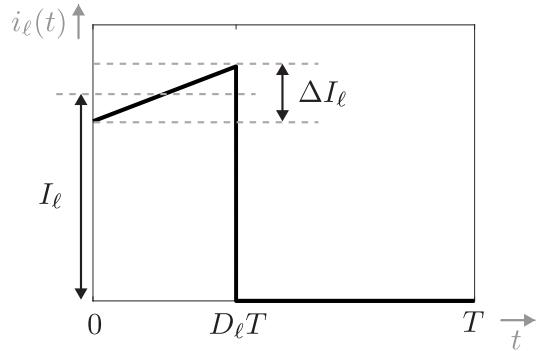


Fig. 8: Time domain sketch of one period of $i_\ell(t)$.

where $\alpha_\ell^k := |\alpha_\ell^k| e^{j\psi_\ell^k}$, with

$$|\alpha_\ell^k| := \frac{1}{2} ((a_\ell^k)^2 + (b_\ell^k)^2)^{\frac{1}{2}}, \quad (8)$$

$$\psi_\ell^k := -\arctan\left(\frac{b_\ell^k}{a_\ell^k}\right). \quad (9)$$

With this in place, let us now derive the Fourier-series coefficients of i_{bus} . We get:

$$i_{bus}(t) = \sum_{\ell=1}^N i_\ell(t) \quad (10)$$

$$= \sum_{\ell=1}^N \sum_{k=-\infty}^{\infty} (\alpha_\ell^k e^{j2\pi kt}) e^{-j\xi_k \theta_\ell}, \quad (11)$$

where θ_ℓ is the phase shift of i_ℓ with reference to an arbitrary reference angle. Note that (10) follows from KCL, while in (11), we have substituted for each i_ℓ from (7), and the factor $e^{-j\xi_k \theta_\ell}$ accounts for the phase shift θ_ℓ [7]. Since i_{bus} and v_{bus} are linearly related by the capacitive impedance, we can obtain the Fourier series of v_{bus} as follows:

$$v_{bus}(t) = \sum_{\ell=1}^N \sum_{k=-\infty}^{\infty} \frac{1}{j2\pi k C_{bus}} \alpha_\ell^k e^{j2\pi kt} e^{-j\xi_k \theta_\ell}. \\ =: \sum_{\ell=1}^N \sum_{k=-\infty}^{\infty} \beta_\ell^k e^{j2\pi kt} e^{-j\xi_k \theta_\ell}. \quad (12)$$

Applying Parseval's theorem [7] and terminating the pertinent summation to some finite $K \in \mathbb{Z}^+$, we get the expression for the ac power corresponding to v_{bus} in (2).