Levelized-Cost-of-Electricity-Driven Design Optimization for Medium-Voltage Transformerless Photovoltaic Converters

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Abstract—Design approaches for power electronics are typically focused on efficiency and power density; however, these strategies do not guarantee cost optimality in any well-defined sense. To overcome this shortcoming, we propose a design framework that yields circuit parameters that minimize the levelized cost of electricity (LCOE) of a generation system. LCOE serves as a meaningful metric since it captures total lifetime costs — including hardware, balance of system, and maintenance costs — and includes the impacts of power conversion efficiency and revenue from harvested energy. To obtain a tractable design problem, we formulate an approximate LCOE improvement model that quantifies the changes in LCOE resulting from a candidate converter design. We apply this framework to a multilevel cascaded topology for low-voltage dc to medium-voltage ac conversion without line-frequency transformers. An example 200 kW commercial-scale system is studied and the solution yields a design with 15 cascaded stages, 98.01 % efficiency, and an LCOE reduction of 2.0 %.

Index Terms—levelized cost of electricity, design optimization, multilevel converters

I. INTRODUCTION

Levelized cost of electricity (LCOE) is a measure to evaluate the net value of a generation system by quantifying the average cost of electricity throughout its lifetime. Since it is expressed in units of energy cost, e.g., $/kWh, it enables a comparison of new technologies to state-of-the-art methods used by industry. In addition, LCOE enables comparison of systems across disparate power levels and different types of generation, such as solar and wind. Due to its versatility, LCOE is widely used to compare existing and new technologies [1]. For instance, the U.S. Department of Energy (DOE) has been using LCOE to

track cost reductions to achieve its target of 3¢/kWh, 4¢/kWh, and 5¢/kWh by 2030 for utility-scale, commercial-scale, and residential-scale PV systems, respectively [2]. Annual LCOE estimates for state-of-the-art practices are benchmarked in [3].

The merit of a given converter design is typically evaluated by a few performance factors. Since efficiency is directly related to energy harvest, it is the most common evaluation criteria [4], [5]. However, efficiency only captures one aspect of the design and might not give insights on how a technology might be commercialized (e.g., cost-effectiveness or reliability). Therefore, it is imperative that systems are evaluated with a comprehensive measure that would most impact the potential for commercialization.

Recently, a new energy-conversion architecture for PV power plants was proposed in [6]. It enables direct low-voltage dc to medium-voltage ac (MVAC) power conversion with cascaded ac-side outputs of string-level inverters. This approach yields a modular system comprised of blocks with decentralized controls and converter circuitry (C^2 blocks), as shown in Fig. 1. The aim of this new concept is to design a system that not only improves efficiency, but also reduces costs by eliminating the low-frequency step-up transformer typically seen in utility and commercial systems to step up and interface inverter's low-voltage ac output to MVAC grid.

Although [6] introduces the C^2-based topology and its controls, it is not yet certain how this new configuration impacts LCOE in comparison to existing designs. To address the gap, this paper proposes an LCOE-oriented approach to optimize the converter design and evaluate its value compared to industry practices. Using the LCOE improvement model developed in this paper, we derive the system-level features (e.g., number of cascaded C^2 blocks) as well as the converter-level circuit parameters (e.g., device ratings, characteristics of semiconductor, and passive components) which minimize LCOE. Section II presents the LCOE improvement model, and Section III discusses the loss and cost models. Section
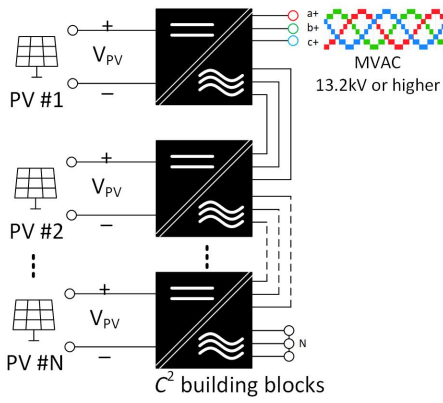
Fig. 1. Multilevel dc to three-phase ac architecture without low frequency transformer. Each C^2 building block interfaces a dc source and three phase ac with isolation and they operate without high fidelity communication.

IV provides details on the LCOE design optimization. An example design for a 200 kW PV system is shown and Section V gives concluding statements.

II. LCOE IMPROVEMENT MODEL

Since the LCOE considers lifetime energy cost of a generation system, it is defined as

$$\text{LCOE} = \frac{C_{\text{life}}}{E_{\text{life}}} \quad (1)$$

where C_{life} is the lifetime cost spent and E_{life} is the lifetime energy yield from a power generation system. LCOE for a PV system can be expressed in the form

$$\text{LCOE} = \frac{C_0 + \sum_{t=1}^{t=T} \frac{C_t}{(1+i)^t}}{8760 \cdot P_{\text{rated}} \cdot \gamma \cdot \left(\sum_{t=1}^{t=T} (1-\delta)^{t-1} \right)} \quad (2)$$

where t is time in years, T is the lifetime of the PV system in years, C_0 is the initial investment cost, C_t is cost incurred at year t, i is the interest rate per period, δ is the PV module degradation factor, e.g., 0.8%/year [7], P_{rated} is the power plant capacity in watt, and $\gamma = c_t \cdot \eta_{PC}$ is the scaling factor, which is the ratio of actual electricity output over a year to the maximum possible output. c_t, capacity factor of a system, depends on geographical location (irradiance and temperature profile) and, in general, ranges from 0.1 to 0.4 [8]. η_{PC} is to represent power conversion efficiency from PV output to AC transmission to detail the inverter performance.

While (2) incorporates several factors which impact cost and energy harvest, it is not straightforward to identify the improvement that a candidate new converter design can achieve compared to an existing baseline design. Towards that end, we denote the LCOE of a *baseline* state-of-the-art technology as

$$\overline{\text{LCOE}} = \frac{\bar{C}_{\text{life}}}{\bar{E}_{\text{life}}} = \frac{\bar{C}_0 + \sum_{t=1}^{t=T} \frac{C_t}{(1+i)^t}}{8760 \cdot P_{\text{rated}} \cdot \bar{\gamma} \left(\sum_{t=1}^{t=T} (1-\delta)^{t-1} \right)}. \quad (3)$$

Using (3), the LCOE of a newly proposed system is written in the form

$$\text{LCOE}_{\text{new}} = \frac{(\bar{C}_0 - \Delta C_0) + \sum_{t=1}^{t=T} \frac{C_t}{(1+i)^t}}{8760 \cdot P_{\text{rated}}(\bar{\gamma} + \Delta\gamma) \left(\sum_{t=1}^{t=T} (1-\delta)^{t-1} \right)} \quad (4)$$

where ΔC_0 and $\Delta\gamma$ are cost and efficiency improvements, respectively, of the proposed design. After neglecting second order terms, (4) can be approximated as the sum of two factors

$$\text{LCOE}_{\text{new}} \approx \overline{\text{LCOE}} - \frac{\Delta C_0}{\bar{E}_{life}} - \overline{\text{LCOE}} \frac{\Delta\gamma}{\gamma}. \quad (5)$$

Finally, we define the LCOE *improvement* factor as

$$\frac{\Delta \text{LCOE}}{\overline{\text{LCOE}}} \approx \frac{\Delta C_0}{\bar{E}_{\text{life}} \overline{\text{LCOE}}} + \frac{\Delta\gamma}{\bar{\gamma}} \quad (6)$$

where $\Delta\text{LCOE} = \overline{\text{LCOE}} - \text{LCOE}_{\text{new}}$. This so-called *improvement model* simplifies calculations since it allows us to isolate the factors which impact LCOE. Incorporating the loss (efficiency) and LCOE data of a baseline approach and improvement factors into (6), the potential improvement in LCOE of a new technology can be computed.

To compute the benefits a new technology can yield in terms of LCOE, this paper assumes that unchanged aspects of the system (e.g., land use) are identical across technologies [9], which allows for reasonable comparison with manageable complexity. Thus, the paper assumes the two systems compared have same capacity factor, degradation factor, interest rates, and maintenance cost. Accordingly, our model captures key changes in losses and cost.

III. MODEL DEVELOPMENT FOR LCOE ANLAYSIS

This section discusses the loss and cost model development of the medium-voltage transformerless PV system reported in [6] to analyze its potential improvement compared to a benchmark technology. To extract the parameters for the baseline, benchmark data annually published by the National Renewable Energy Laboratory is used [3].

A. Medium-Voltage PV System Using C^2 Building Blocks

The new topology under consideration in Fig. 2 has a quadruple-active-bridge (QAB) operated as a dc transformer (DCX); local dc-link controllers regulate dc-link voltages at $n \cdot v_k^{PV}$, where n is the tranformer turns ratio and v_k^{PV} is the PV input voltage of the kth block. On the output side, three single-phase inverters interface to grid with multiple C^2 blocks connected in series across the grid. To obtain a model for converter costs and losses, we must first outline the operational and physical characteristics of the circuit in Fig. 2.

The QAB can take the form of three dual-active-bridges (DABs) operated as three DCXs to regulate the three dc link voltages at $n \cdot v_k^{pv}$; each dc-link controller regulates its dc link voltage independently by phase-shift modulation while primary-side pulse width modulation (PWM) is fixed. The DCX approach restricts operation to regimes where efficiency is maximum [10]. Each set of three single-phase inverters on the output ac-side are controlled to conduct maximum power
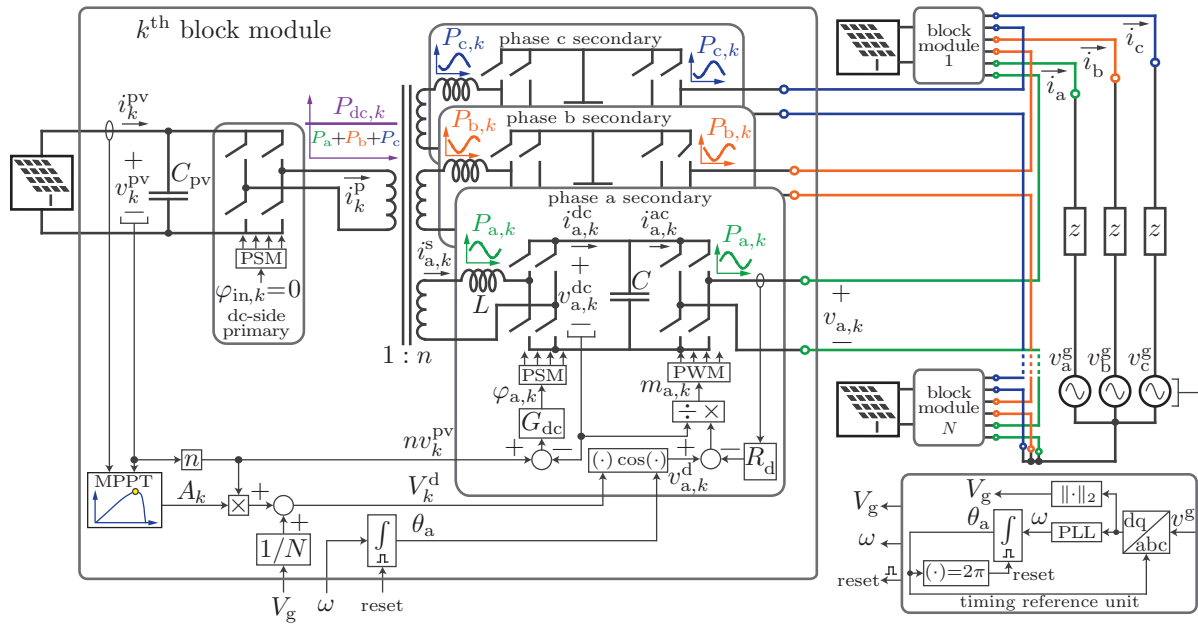
Fig. 2. C^2 Building block circuit diagram and its control [6].

point tracking (MPPT) and ensure voltage balancing between series modules via droop control (see details in [6]). The stacked modules are interleaved to produce $2N + 1$ voltage levels (N is the number of series blocks) to minimize output filtering requirements in decentralized fashion [11]. Since the pulsating double frequency ($2\omega_{grid}$) power processed by each DAB sums to a constant dc value on the PV input side, i.e., $n\left(\langle i_{a,k}^{dc}\rangle + \langle i_{b,k}^{dc}\rangle + \langle i_{c,k}^{dc}\rangle\right) = i_k^{pv}$ in balanced system, this architecture does not require large decoupling capacitors (unlike MMCs and other approaches which require sizable decoupling capacitors [12]). Since multilevel operation reduces the ac-side filter size, we assume that the loss and cost of the output filters are negligible. Now we proceed to the loss and cost models which underpin the LCOE optimization design framework. All loss and cost models are designed to be *scalable* by optimization method to derive optimal design values.

B. Loss Models

With the assumption that the majority of loss occurs in power conversion stages, switch device loss and magnetic loss of inductor and transformer are the major loss factors for the C^2 blocks.

1) Switch Loss: Switch loss consists of conduction and switching loss. Switch conduction loss can be formulated as

$$
\begin{aligned}
P_{\text{loss,SW,cond}} = {}& 4 \cdot i_{\text{rms,pri}}^2 R_{\text{ds,pri}} \\
& + 3 \cdot 4 \cdot i_{\text{rms,sec}}^2 R_{\text{ds,sec}} + 3 \cdot 4 \cdot i_{\text{rms,inv}}^2 R_{\text{ds,inv}}
\end{aligned}
\tag{7}
$$

where $i_{\text{rms,pri}}$, $i_{\text{rms,sec}}$, $i_{\text{rms,inv}}$, $R_{\text{ds,pri}}$, $R_{\text{ds,sec}}$, and $R_{\text{ds,inv}}$ are switch rms currents and on-resistances on the DAB primary, secondary, and inverter sides, respectively. Since the primary

side of QAB delivers dc current without line frequency component, the primary-side current can be approximated as

$$
i_{\text{rms,pri}} \approx \frac{i_k^{pv}}{1 - \frac{\phi_{\max}}{\pi}} \sqrt{\frac{1}{2} - \frac{\phi_{\max}}{3\pi}}
\tag{8}
$$

where $\phi_{\max}$ is the maximum phase shift for the rated power. The secondary-side switch rms current can be also derived similarly considering the sinusoidal output current as

$$
i_{\text{rms,sec}} \approx \frac{v_{a,k}^{dc} \cdot \phi_{\max}}{2\pi \cdot f_{s,\text{DAB}} \cdot L} \cdot \sqrt{\frac{1}{4} - \frac{4\phi_{\max}}{9\pi^2}}
\tag{9}
$$

where $f_{s,\text{DAB}}$ is the switching frequency of QAB and L is the leakage inductance of the transformer on secondary side designed to match with $\phi_{\max}$ at rated power. The rms current for inverter stage can be also derived considering the inverter modulation [13].

Switching loss of the devices are modeled under soft-switching conditions. With a given deadtime, the operating points which give zero voltage switching (ZVS) for the DABs and the three single-phase inverters can be derived. For simplicity, this paper considers mild-ZVS (partially discharged parasitic capacitance) as hard-switching, which leads conservative estimation of efficiency. The switching loss of the primary side switches can be modeled by identifying $i_{\text{ZVS,min}}$ which is minimum current needed to fully discharge/charge parasitic capacitance with given deadtime. Since primary side of the QAB carries dc current, switching loss is estimated as either 0 for ZVS case or $2 \cdot C_{\text{oss,pri}} v_{a,k}^{2dc}$ for hard-switching case. The ZVS condition of secondary side switches can be found considering the sinusoidal output current as

$$
P_{\text{sw,sec}} = 2k C_{\text{oss,sec}} v_{a,k}^{2dc} f_{s,\text{DAB}}
\tag{10}
$$

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where,

$$k = \frac{2}{\pi} \sin^{-1}\left(\sqrt{\min\left(\frac{i^s_{i,k,zvs}}{i^s_{i,k,peak}}, 1\right)}\right) \quad (11)$$

$i^s_{i,k,zvs}$ is the minimum average current value to achieve ZVS on secondary side, and $i^s_{i,k,peak}$ is the peak current on the secondary side. The switching loss of inverter switches can be also modeled by considering modulation method [13].

To obtain a scalable model that is written in terms of independent design variables (i.e., ratings), a simplified device model calibrated with commercial bare die data from Cree Wolfspeed is used. As shown in [14] the specific on resistance of a vertical MOSFET may be approximated as shown in (12) as long as the drift region resistance is the dominant component of the on-resistance.

$$R_{\text{ds,sp}} = K_{\text{SiC}} V_{\text{BD}}^{\kappa} \quad (12)$$

where κ depends on the semiconductor process and, in general, ranges from 2 to 3 [14] which implies the benefit of multilevel topologies.

The area of the device may then be determined given a desired on-resistance. The output capacitance of the device may then be estimated by assuming that capacitance can be approximated by a parallel plate capacitor that whose height, (14), is set by the desired breakdown voltage and a fixed capacitance that does not depend on the dimensions of the device.

$$C_{\text{oss}} = \epsilon \frac{A_{\text{die}}}{W_{\text{d}}} + C_{\text{fixed}} \quad (13)$$

$$W_{\text{d}} = 2\frac{V_{\text{BD}}}{E_{\text{C,SiC}}} \quad (14)$$

2) Magenetic Loss: In general, magnetic loss factors of the DAB transformer and leakage inductor are represented by core and winding loss. Core loss is characterized by the iGSE method [15] to generate an accurate estimation for non-sinusoidal voltage excitations. The core loss can be estimated as

$$P_{core} = \frac{1}{T_s} \int_0^{T_s} \frac{K_{fe}}{2\pi^{\alpha-1} \int_0^{2\pi} |\cos\theta|^2 2^{\beta-\alpha} d\theta} |B(t)|^{\beta-\alpha} \left|\frac{dB}{dt}\right|^{\alpha} dt \quad (15)$$

where K_{fe}, β, and α are extracted from the datasheet. A PLECS simulation is integrated into the optimization platform to provide the total flux linkage fed to the model to generate the flux density profile, $B(t)$. Here we consider planar magnetics with PCB trace windings. Given a core geometry, we produce the following scalable conduction loss model that incorporates dc resistance, skin effect, and proximity effect. Using Dowell's equation to solve for conduction loss in a particular layer [16]:
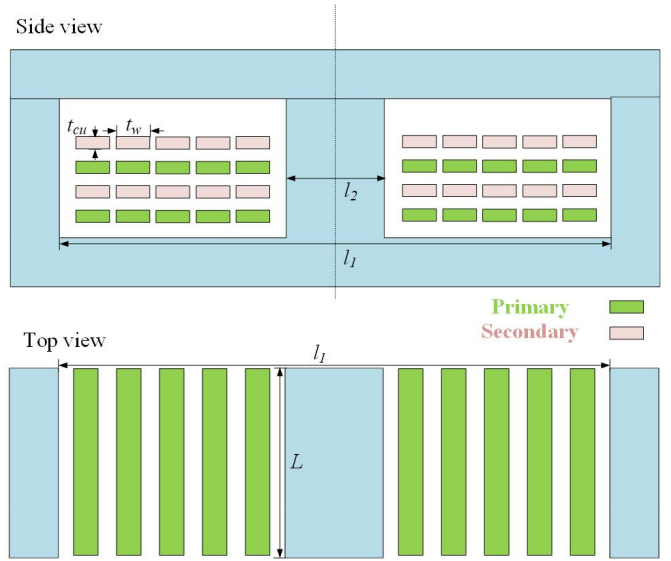

Fig. 3. 2D drawing marking important dimensions for an example interleaved transformer with $N = 10$ and $m = 2$.

$$P_{layer} = \frac{R_{dc}\phi}{(N/m)^2}\left(\left(f_h^2 + f_0^2\right)\left(\frac{\sinh(2\phi) + \sin(2\phi)}{\cosh(2\phi) - \cos(2\phi)}\right)\right.$$
$$\left. - \left(4\left(\frac{\sinh(\phi)\cos(\phi) + \cosh(\phi)\sin(\phi)}{\cosh(2\phi) - \cos(2\phi)}\right)f_h f_0\right)\right) \quad (16)$$

where $R_{\text{dc}} = \rho\frac{MLT}{t_w t_{cu}}$, N/m is turns per layer (N: total turns, m: number of layers on primary or secondary), $MLT = 2L + \pi\frac{l_1+l_2}{2}$ is mean length per turn, t_{cu} and t_{w} are copper thickness and width (refer Fig. 3 for graphical explanation), and $\varphi = t_{\text{cu}}/\delta$ with $\delta = (\rho/(\pi\mu_0 f_{DAB}))^{0.5}$ for skin effect. $f_h = f_0 + nI$, where I is the harmonic currents; f_h and f_0 are recursively calculated to represent the impact of current harmonics. With a given volume, the model results in optimal PCB copper thickness, number of layers, and winding turns. This paper uses the material of TDK ELP series core and N87 material for analysis. Using this model, core and winding loss are scaled by volume and voltage/current parameters which are varied by the solver. ANSYS Maxwell, a finite element analysis (FEA) software package, was used to validate model accuracy.

3) Cost Model: While the scalable loss model is relatively straightforward considering loss mechanism, reliable cost model development is challenging due to a variety of factors that may affect its reliability, e.g., inconsistent market prices and installation labor costs. To address the challenges, this study employs a comparative cost approach which quantifies relative improvements. Regarding the inverter cost model, this allows us to neglect components, such as enclosures and auxiliary circuitry, which are similar between the C^2 architecture and baseline state-of-the-art approaches. Hence, we confine analysis to key components which are distinct [17]. This assumption simplifies the cost model of
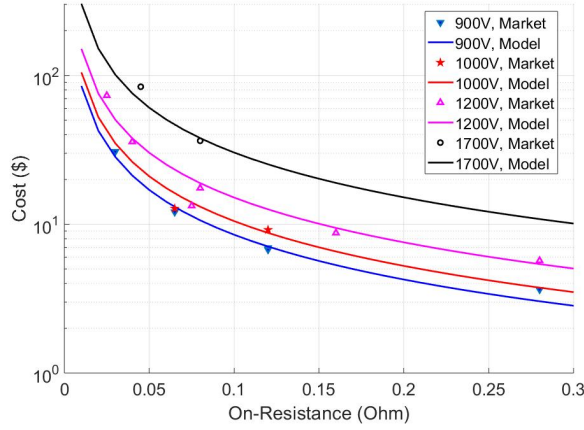
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Fig. 4. Semiconductor cost model for CREE Wolfspeed SiC switches.

the architecture and allows us to focus on semiconductor and magnetic component cost models and their associated impacts on relative cost improvements.

Market data are used to generate the scalable cost models for semiconductors and magnetic devices. Using the scalable models, one can estimate the cost for arbitrary switch and magnetic devices. To build the switch cost model, cost data of CREE Wolfspeed SiC devices ranging from 900 V to 1700 V are extracted. This modeling effort is to capture cost changes with different on-resistances and breakdown voltages. It is intuitive to expect that the switch cost will be proportional to semiconductor die area, and referring to the earlier discussion and (12), it can be expressed as

$$C_{\text{semi}} = k_{\text{semi,cost}} \cdot \frac{V_{\text{BV}}^{\kappa}}{R_{\text{ds}}}. \qquad (17)$$

Fig. 4 compares semiconductor cost model and market data. The scalable cost model reasonably traces the market cost trends while it shows errors that may result from device availability and popularity of specific voltage and current capacity variations.

Magnetic core cost model is built from the core volume and market data that leads a volume-scaled model. Since the purpose of the modeling is to capture cost trend of the magnetic devices with different core volume, it is assumed that the core volume can be fully scaled given an aspect ratio, and TDK ELP 102 core is set as baseline for the optimization; k_{core} serves as a scaling factor.

IV. LCOE OPTIMIZATION

A. Optimization Framework

Based on the loss and cost models built in Section III, the LCOE improvement model to solve the optimization problem is developed. To complete the comparison model in (6), the

LCOE benchmark data [3] is used to compute ΔC_0 and $\Delta \gamma$. Incorporating the data and cost models yields

$$
\begin{aligned}
\Delta C_0 &= \Delta C_{0,\text{trans}} + \Delta C_{0,\text{semi}} \\
&= (C_{\text{trans,bench}} - C_{\text{trans},C^2}) + (C_{\text{semi,bench}} - C_{\text{semi},C^2}) \quad (18)
\end{aligned}
$$

where $\Delta C_{0,\text{trans}}$ is the cost improvement by employing high frequency magnetics instead of low frequency transformers, and $\Delta C_{0,\text{semi}}$ is the improvement in semiconductor cost from baseline. Both improvement factors can be either positive or negative depending on the design. The two benchmark cost data, $C_{\text{trans,bench}}$ and $C_{\text{semi,bench}}$, are extracted from the balance of system (BOS) cost benchmark and inverter cost analysis. Since the benchmark data only includes the inverter cost without further details, e.g., cost of semiconductor switches, [17] is referred to derive cost proportion of semiconductors. As the use of SiC devices is envisioned in this approach, benefits from high switching frequency operation in filter size reduction and thermal management are considered. Benefits of multilevel operation and reductions in filter requirements can be also included in this model.

Energy yield improvement from inverter efficiency can be derived as

$$\Delta \gamma = \gamma - \bar{\gamma} = c_t(\eta_{\text{PC},C^2} - \eta_{\text{PC,bench}}). \qquad (19)$$

Considering the same geographic location for fair comparison, the power conversion efficiency drives the improvement. Based on the DOE benchmark, 98% inverter efficiency for the baseline is used for the analysis while 99% efficiency of energy-efficient line frequency transformer is assumed based on the U.S. Department of Energy Efficiency Standards: Low Voltage Distribution Transformers, DOE-2016 [18]. To further detail the loss factors, additional factors can be considered including the downtime for maintenance and potential additional energy yield from modular approach.

Regarding the other factors in (6), we use the LCOE baseline [3] for average commercial PV generation system with 30% investment tax credit and 0.7% annual degradation of the PV module is considered. A 1000 VDC PV array is assumed, but the model can be used to study the effect of other PV voltages, e.g., 1500 VDC that is being adapted for high efficiency power conversion. A 13.2-kV three-phase grid is assumed for the medium voltage interface.

B. Case Study: Optimization of C^2 system for 200-kW

To estimate the improvement from the C^2 architecture, we consider a case study of 200-kW commercial inverter system. With the fixed system power capacity, the optimization model shown in Fig. 5 derives maximum LCOE improvement with an optimization method. This paper uses a brute-force method to exhaustively explore the entire potential design spaces and it can be used for further development as baseline. Once the range of three high-level scalable design parameters are defined, the other parameters are determined and model outputs loss and cost. Given all potential design variations, optimal design parameters for maximum LCOE improvement
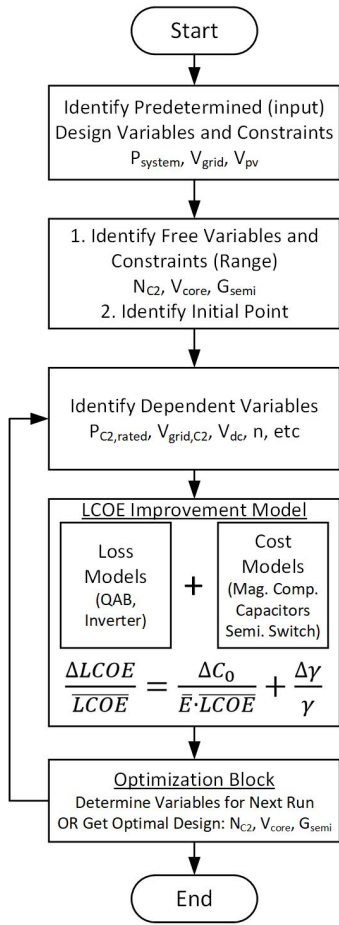
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Fig. 5. LCOE-driven design optimization framework.

Fig. 6. LCOE improvement with different number of modules and switch on-resistances at fixed core volume, $k_{core} = 3$.

Fig. 7. Loss factor varying with different designs. $k_{core} = 3$.

are identified to provide insights to be used for system design. Though it assumes the switching frequency is fixed, 100 kHz in this paper, it can be also incorporated in the framework.

LCOE optimization results using the exhaustive method are shown. The LCOE improvement plot in Fig. 6 with different on-resistance and module numbers and fixed core volume, k_{core}=3 indicates LCOE is heavily affected by inverter design. This graphical approach provides intuitions for optimal design balancing the trade-off between efficiency and cost. For instance, it clarifies a trend in LCOE heavily affected by transformer turns ratio causing step changes in switch device voltage ratings; a smaller number of series modules necessitate higher voltage rated devices to sustain the same grid voltage. As expected, use of high voltage devices leads worse figure of merit of switches and, as a result, less favorable switching and conduction loss trade-off and as well as increased cost as implied in (12) and (17). Figs. 7 and 8 displays total loss and cost characteristics on the design space, respectively. Note that the optimal point is not the least loss design nor the design with least \$/W cost. In addition, Fig. 9 illustrates impact of core volume on magnetic loss factor. Similar to the previous observation, the module number would heavily
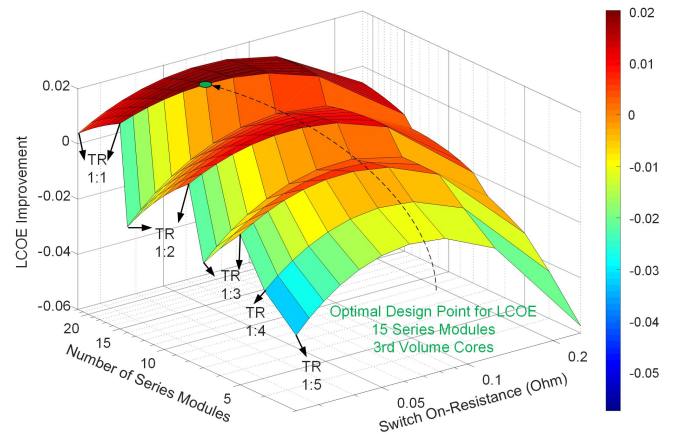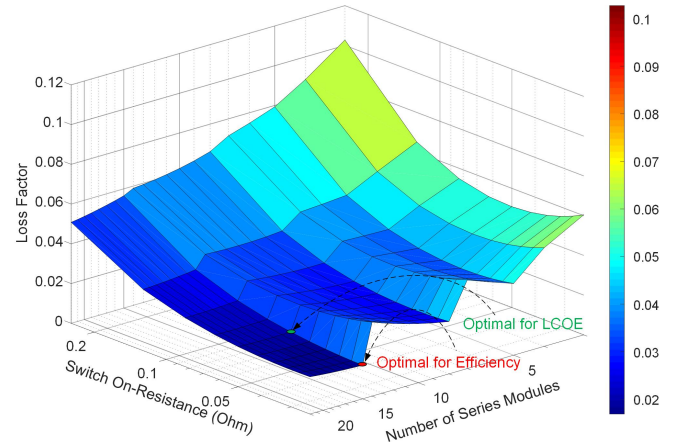
impact the loss and, as a result, LCOE. Fig. 10 illustrates impact of on-resistance and core volume on LCOE with 15 C^2 modules. As expected from previous discussion, balanced design parameters yield maximum LCOE improvement.

Our approach illuminates the interplay between efficiency and costs that give the lowest LCOE. Under the case study considered here, the 200-kW PV system can improve LCOE by 2.0% with 15 cascaded C^2 modules, 50 $m\Omega$ SiC devices and transformers with $k_{core} = 3$ that leads an efficiency of 98.01% compared to the state-of-the-art practices. Although the exhaustive optimization method used in this paper provides design insights capturing important loss and cost factor trends depending on the high-level parameters, the optimal design derived may be coarse due to computation limit or requires repetitive iteration for fine result. To overcome this limit, advanced optimization methods such as convex and genetic algorithm can be applied. To fit into these advanced methods, additional steps, e.g., formulating the models into convex optimization problem to obtain convexity, may be required. If successful, additional key design variables including switching
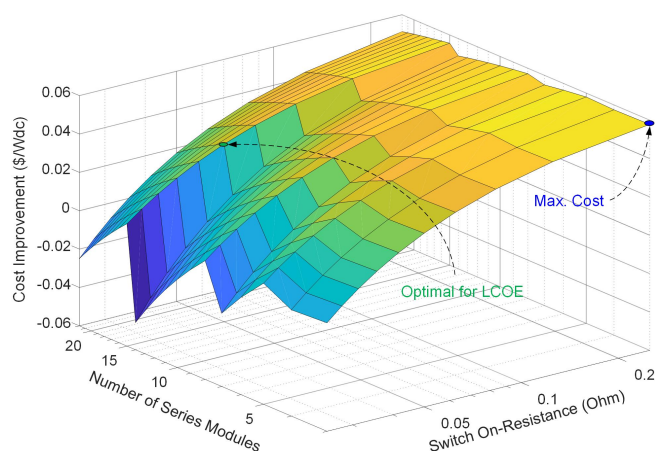
Fig. 8. Cost improvement with on-resistance and module number variations. Maximum cost improvement does not match with optimal for LCOE.
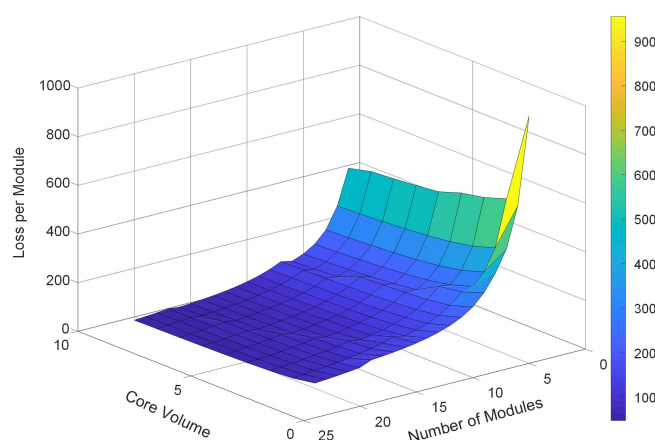

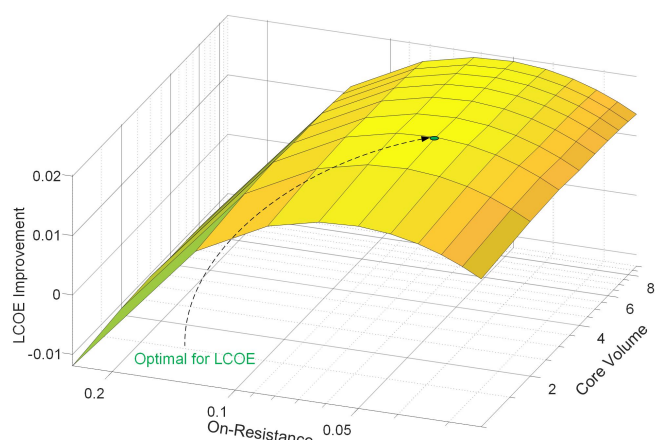Fig. 9. Magnetic loss per module with varying module numbers and core volume.

Fig. 10. LCOE improvement with on-resistance and core volume varying.

frequency in addition to fine results would be achieved.

V. CONCLUSION

This paper presents a novel LCOE improvement model for PV system architectures, which may serve as the basis of a design procedure for complex power electronics systems in general. This approach allows for the comparison of a candidate converter design to existing state-of-the-art systems. Our model streamlines analysis and allows us to isolate the distinct components to drive impacts on LCOE. Model fidelity can be enhanced to incorporate additional components of interest. To exemplify the approach, a comprehensive model formulation is provided for a PV system architecture using multilevel cascaded converter blocks for low-voltage dc to medium-voltage ac conversion without line-frequency transformers. A case study of a 200-kW PV system shows 2.0% potential LCOE improvement using an optimized architecture.

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REFERENCES

[1] K. Branker, M. Pathak, and J. M. Pearce, "A review of solar photovoltaic levelized cost of electricity," *Renewable and sustainable energy reviews*, vol. 15, no. 9, pp. 4470–4482, 2011.

[2] SunShot Initiative, "Sunshot Vision Study," tech. rep., U.S. Department of Energy, 2012.

[3] R. Fu, D. Feldman, and R. Margolis, "US solar photovoltaic system cost benchmark: Q1 2018," tech. rep., National Renewable Energy Laboratory, 2018.

[4] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 184–191, 2009.

[5] A. Stupar, M. Halamicek, T. Moiannou, A. Prodic, and J. A. Taylor, "Efficiency optimization of a 7-switch flying capacitor buck converter power stage IC using simulation and geometric programming," in *proc. IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–8, 2018.

[6] P. K. Achanta, B. B. Johnson, G.-S. Seo, and D. Maksimovic, "A multilevel dc to three-phase ac architecture for photovoltaic power plants," *IEEE Transactions on Energy Conversion*, vol. 34, no. 1, pp. 181–190, 2018.

[7] D. C. Jordan and S. R. Kurtz, "Photovoltaic degradation ratesan analytical review," *Progress in photovoltaics: Research and Applications*, vol. 21, no. 1, pp. 12–29, 2013.

[8] Energy Information Administration (EIA), "Electric power monthly-with data for april 2019," tech. rep., U.S. Department of Energy, 2019.

[9] S. B. Darling, F. You, T. Veselka, and A. Velosa, "Assumptions and the levelized cost of energy for photovoltaics," *Energy & Environmental Science*, vol. 4, no. 9, pp. 3133–3139, 2011.

[10] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson, and D. Maksimovic, "A 98.7% efficient composite converter architecture with application-tailored efficiency characteristic," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 101–110, 2015.

[11] S. Dutta, R. Mallik, B. Majmunovic, S. Mukherjee, G.-S. Seo, D. Maksimovic, and B. Johnson, "Decentralized carrier interleaving in cascaded multilevel dc-ac converters," in *proc. Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–6, 2019.

[12] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *proc. IEEE Bologna Power Tech Conference*, vol. 3, pp. 1–6–pp, 2003.

[13] C. L. Nge, O.-M. Midtgård, L. Norum, and T. O. Sætre, "Power loss analysis for single phase grid-connected PV inverters," in *proc. International Telecommunications Energy Conference (INTELEC)*, pp. 1–5, 2009.

[14] N. Mohan and T. M. Undeland, *Power electronics: converters, applications, and design*. John wiley & sons, 2007.

[15] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *proc. IEEE Workshop on Computers in Power Electronics*, pp. 36–41, 2002.

[16] R. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Springer, 2001.

[17] U. Schwarzer, S. Buschhorn, and K. Vogel, "System benefits for solar inverters using SiC semiconductor modules," in *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management(PCIM Europe)*, pp. 1–8, VDE, 2014.

[18] D. Garcia, J. Valencia, and G. Hausman, "U.S. Department of Energy 2016 transformer efficiency changes and impact on inrush current for low voltage dry-type transformers," tech. rep., Eaton, 2016.