Soft Switching Over the Entire Line Cycle for a Quadruple Active Bridge DCX in a DC to Three-Phase AC Module

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Abstract—This paper is focused on a transformer-isolated quadruple active bridge (QAB) dc-dc converter loaded by three full-bridge dc-ac inverters. The QAB functions as a "DC transformer" (DCX) in the dc-to-three-phase ac module. The QAB outputs provide time-varying power at twice the line frequency, which presents challenges in maintaining zero voltage switching (ZVS) on the secondary sides during low-power portions of the line cycle. It is shown how ZVS can be achieved in a phase, even at zero-power transfer, using a relatively small circulating current provided by the magnetizing inductance of the high-frequency transformer. The approach is particularly effective in high-voltage applications using SiC MOSFETs, where reductions in switching loss outweigh additional conduction losses due to the circulating currents. A detailed analysis of ZVS switching waveforms at the zero power transfer is presented, including effects of nonlinear device capacitances. Analytical expressions are given for the optimal values of the magnetizing inductance and dead times of the QAB primary and secondary bridges. The approach is verified by experimental results on a 600 V, 4 kW prototype, demonstrating greater than 98.5% efficiency from 1 kW to 4 kW, with a peak efficiency of 99.0%. Compared to conventionally operated prototype, a 54% reduction in total loss is achieved at rated power.

I. INTRODUCTION

Dc-to-three-phase-ac converters, with isolation between the phases, unlock the flexibility to create scalable, modular architectures with either parallel, or series interconnections. Here, we consider the modular photovoltaic (PV) system in Fig. 1, where each dc input is supplied from a PV string and the ac outputs are cascaded in series to achieve elevated voltages without a line-frequency transformer [1]. As shown
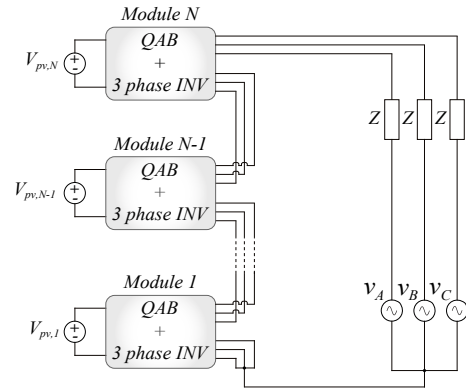
Fig. 1: Photovoltaic (PV) system architecture with cascaded isolated inverter modules [1].

in Fig. 2, each isolated module contains a quadruple active bridge (QAB) followed by three dc-ac inverter bridges. The QAB, which operates as a "DC transformer" (DCX), provides galvanic isolation between the primary and each of the individual ac phases so they can be flexibly stacked on the ac side.

Three-phase ac power flows through the three secondaries of the QAB. The QAB outputs connected to phases A, B, and C deliver time-varying power $p_A(t)$, $p_B(t)$, and $p_C(t)$, respectively, each having a dc and double-line-frequency ac component. The three currents sum up on the primary side, such that smooth dc power is transferred from the input, and dc-link capacitance requirements are relaxed. The fact that the power fluctuates from zero to twice the average power on each secondary during a line cycle presents challenges with respect to soft-switching of the secondary side bridges. This is similar to loss of zero-voltage switching (ZVS) in lightly loaded dual-active-bridge dc-dc converters where inductively stored energy is insufficient to achieve soft charging and discharging of the
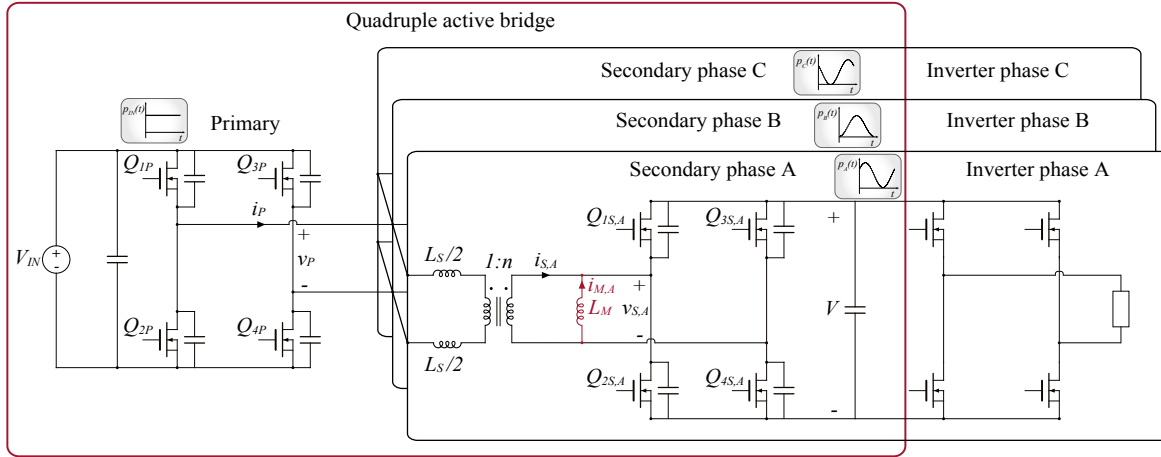
Fig. 2: Transformer-isolated inverter module using quadruple active bridge (QAB) dc-dc converter operated as DCX.

switching-node capacitance [2], [3]. This capacitance consists of power MOSFET capacitances, winding capacitance, and printed circuit board (PCB) parasitic capacitance.

Dual active bridge (DAB) converters have been used in applications that process ac power such as ac-dc rectifiers [4]–[6] and ac-ac [7] converters. A modulation strategy for operating DABs under soft switching conditions throughout the entire operating range was proposed in [8], but the effects of the device output capacitances were not fully taken into account. The work in [2] showed that reduced magnetizing inductance can lead to an extended ZVS range, but interactions between the magnetizing inductance and the device output capacitances were not addressed. Utilization of the transformer magnetizing current to extend ZVS to light load region was also proposed in [9], [10]. This approach relies on relatively complex high-resolution dead-time control to account for multiple resonant periods, which in practice may result in loss of ZVS. Facilitating ZVS transitions by utilizing magnetizing current was also discussed in [11] for a DCX based on a series resonant converter (SRC).

Unique to the QAB stage shown in Fig. 2, the primary-side power is dc, which means that ZVS can be accomplished throughout the line cycle on the primary bridge. However, the loss of ZVS on the secondary side during low-power intervals of an ac line period results in reduced system efficiency. This paper proposes a solution for ZVS operation of the QAB over the entire ac line cycle by utilizing the magnetizing currents of the transformers (or separate auxiliary inductors), as illustrated in Fig. 2. By reducing the magnetizing inductance of the transformer, circulating currents are introduced through the secondary sides of the QAB. The circulating currents greatly reduce switching loss at the cost of slightly increased conduction loss. A design procedure is developed to select the converter parameters to minimize the circulating currents, while maintaining ZVS even when a phase operates at zero instantaneous power transfer. The operating point corresponding to zero power transfer in one of the three phases is discussed
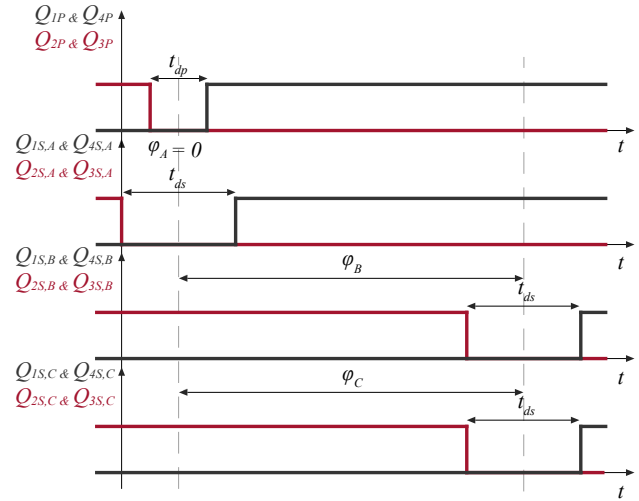

Fig. 3: QAB switch control signals at the time when the secondary Phase A processes zero power.

in detail, and approximate closed form expressions are found for choosing the magnetizing inductance and the dead times. The nonlinear nature of the device parasitic capacitances is taken into account based on the approach described in [12]. Using simple phase shift modulation the QAB is closed-loop controlled as a triple-output DCX.

II. ZERO VOLTAGE SWITCHING AT ZERO INSTANTANEOUS POWER TRANSFER IN ONE PHASE

To guarantee ZVS operation of a particular phase over the entire line cycle, it is sufficient to show how ZVS can be achieved at the zero power transfer instant. The solution presented in this section is based on sizing the magnetizing inductance and a proper combination of the primary and secondary-side dead times.

Consider the time instant when the power processed by phase A is zero, while phases B and C contribute non-zero instantaneous power levels to maintain constant overall power in the three-phase module. The corresponding switch control
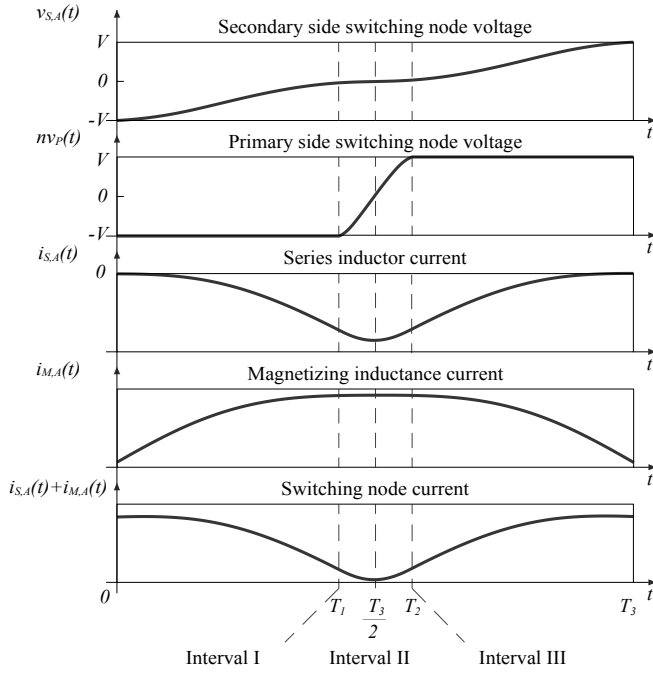
Fig. 4: Model-based waveforms of the ZVS transition at the zero power transfer instant for Phase A. Referring to Fig. 3, $T_3 = t_{ds}$ and $T_2 - T_1 = t_{dp}$.

signals are shown in Fig. 3. The phase shift φ_A between the primary bridge and the phase A secondary bridge is zero, so that the corresponding control pulses are centered around the same instant. Theoretical, model-based waveforms during the rise-time transition of the secondary switching node are shown in Fig. 4. Definitions of the time instants and the time intervals during the transition are given in Tables I and II, while the corresponding equivalent circuit models for the switching sequence consisting of Intervals I, II and III are shown in Fig. 5.

Table I:
Time instants of the switching
sequence during ZVS transition

T_1	$0.5(t_{ds} - t_{dp})$
T_2	$0.5(t_{ds} + t_{dp})$
T_3	t_{ds}

Table II:
Time intervals of the switching
sequence during ZVS transition

Interval I	$0 \le t < T_1$
Interval II	$T_1 \le t < T_2$
Interval III	$T_2 \le t < T_3$
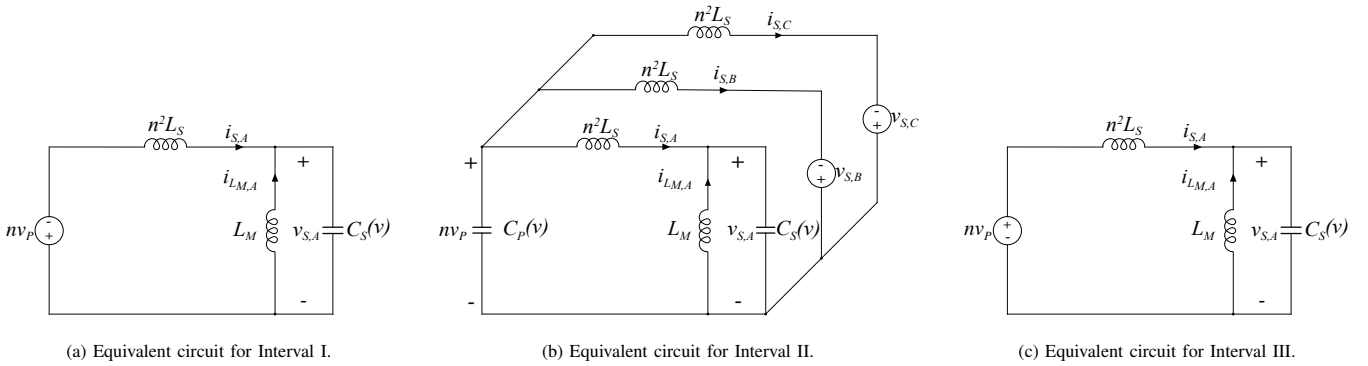
At the beginning of time Interval I (Fig. 5(a)), the secondary side switches $Q_{2S,A}$ and $Q_{3S,A}$ are turned off. The magnetizing inductance current $i_{M,A}$ starts charging voltage dependent switching-node capacitance $C_S(v)$ of the phase A secondary bridge, and the switching node voltage $v_{S,A}$ starts increasing. As $v_{S,A}$ increases, a negative voltage is applied across the series inductance, and the current $i_{S,A}$ starts decreasing.

The primary-side switches Q_{2P} and Q_{3P} turn off at the beginning of Interval II. The equivalent circuit in Interval II is shown in Fig. 5(b). During this interval, phases B and C are charging the switching-node capacitance $C_P(v)$ on the primary side. It is assumed that the QAB is closed-loop controlled to operate as a DCX, so that $v_{S,B}$ and $v_{S,C}$ can be considered constant voltage sources. The rise time of the primary side switching node v_P is faster than $v_{S,A}$, because the sum of the currents $i_{S,B}$ and $i_{S,C}$ is much higher than the peak of the magnetizing current. At the mid-point of Interval II, nv_P becomes higher than $v_{S,A}$, and $i_{S,A}$ changes polarity. Interval II ends, completing the ZVS transition of v_P, at the end of the primary-side dead time t_{dp}.

Interval III starts with turning on switches Q_{1P} and Q_{4P} of the primary full bridge. The corresponding equivalent circuit is shown in Fig. 5(c). During this interval, current $i_{S,A}$ is increasing until $v_{S,A}$ reaches the end of the ZVS transition. At that instant, $Q_{1S,A}$ and $Q_{4S,A}$ are turned on, which ends Interval III and the secondary phase A dead time t_{ds}.

It should be noted that the sum of the magnetizing and series inductance current ($i_{M,A} + i_{S,A}$) reaches a minimum in the middle of Interval II. If this current becomes negative, it will start discharging the secondary side switching-node capacitance $C_S(v)$, which means that it would not be possible to complete the ZVS switching sequence as described above. Fig. 4 shows theoretical waveforms for the case when the minimum of ($i_{M,A} + i_{S,A}$) is zero. This represents the optimal design, in the sense of achieving ZVS operation while minimizing peak of the magnetizing inductance current, and therefore minimizing the conduction losses introduced by the circulating current.

(a) Equivalent circuit for Interval I.

(b) Equivalent circuit for Interval II.

(c) Equivalent circuit for Interval III.

Fig. 5: Equivalent circuits during ZVS transition at the zero power transfer instant for one of the phases.

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P	Rated power
V	DC link voltage
n	Transformer turns ratio
f_{sw}	Switching frequency
φ_m	Maximum phase shift

III. PARAMETER SELECTION FOR MINIMUM PEAK MAGNETIZING CURRENT

In order to achieve ZVS at zero power transfer, the following circuit parameters need to be determined:

- Primary dead time: t_{dp}
- Secondary dead time: t_{ds}
- Magnetizing inductance referred to the secondary side: L_M.

In the design approach detailed in this section, all the parameters are expressed in terms of the specifications and the circuit parameters shown in Table III.

The series inductance

$$L_S = \frac{3V^2\varphi_m\left(1 - \frac{\varphi_m}{\pi}\right)}{4\pi n^2 f_{sw} P} \tag{1}$$

and the peak value of the primary side current

$$I_{P,pk} \approx \frac{nP}{V\left(1 - \frac{\varphi_m}{\pi}\right)} \tag{2}$$

are found using the standard steady-state solution for the active-bridge converters [1].

A. Nonlinear switching node capacitance

In the small-signal sense, the device capacitance "seen" at the half-bridge switching node is a parallel combination of the two device output capacitances, $C_{oss,hb}(v) = (C_{oss}(v) + C_{oss}(V_A - v))$, as shown in Fig. 6, where $C_{oss}(v)$ curve can be found from the device datasheet, and V_A is the dc voltage across the half-bridge. The total half-bridge switching node capacitance is a combination of the device capacitances, winding capacitance, PCB parasitic capacitance:

$$C_{hb}(v) = C_{oss,hb}(v) + C_w + C_{PCB}. \tag{3}$$

The half-bridge capacitances of the primary and the secondary side are denoted as $C_{P,hb}(v)$ and $C_{S,hb}(v)$, respectively. For the equivalent circuit representation used in Fig. 5 and Fig. 7, it is convenient to define full-bridge switching node voltage dependent capacitances as $C_P(v) = C_{P,hb}(v)/2$ for the primary, and $C_S(v) = C_{S,hb}(v)/2$, for the secondary sides.
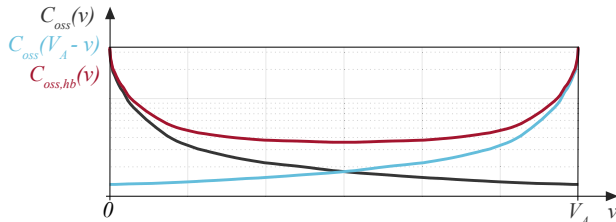

Fig. 6: Half-bridge switching node device capacitance.

The energy and charge equivalent primary-side full-bridge switching-node capacitance are found, respectively, as follows [12]

$$C_{P,E} = \frac{n^2\int_0^{\frac{V}{n}} vC_{P,hb}(v)dv}{V^2} \tag{4}$$

$$C_{P,Q} = \frac{n\int_0^{\frac{V}{n}} C_{P,hb}(v)dv}{2V}. \tag{5}$$

The analysis in Section III-C considers only one half of the secondary side ZVS transition. Consequently, the energy equivalent secondary-side full-bridge switching-node capacitance is obtained by integration up to one half of the dc link voltage

$$C_{S,EH} = \frac{4\int_0^{\frac{V}{2}} vC_{S,hb}(v)dv}{V^2}. \tag{6}$$

B. Primary side dead time

Since the sum of the currents $i_{S,B}$ and $i_{S,C}$ is much greater than $i_{M,A}$, the rise time of the primary side switching node can be analyzed neglecting the effect of the phase A secondary side current $i_{S,A}$. Therefore, the equivalent circuit in Fig. 5(b) can be reduced to a simple LC circuit. Charge equivalent capacitance can be used to accurately calculate the switching-node voltage rise time, under the assumption that the energy stored in the series inductor is much higher than the energy used for charging the switching-node capacitance

$$I_{P,pk} \gg \frac{2V}{n}\sqrt{\frac{C_{P,E}}{L_S}} \tag{7}$$

or, equivalently

$$P \gg \frac{16\pi f_{sw}C_{P,E}V^2}{3n^2\varphi_m}\left(1 - \frac{\varphi_m}{\pi}\right). \tag{8}$$

Consequently, primary-side dead time can be found as

$$t_{dp} = \frac{2VC_{P,Q}}{nI_{P,pk}} = \frac{2C_{P,Q}V^2}{n^2 P}\left(1 - \frac{\varphi_m}{\pi}\right). \tag{9}$$

C. Magnetizing inductance and secondary-side dead time

The switching sequence, described in Section II, involves equivalent circuits shown in Fig. 5. Exact solution is complicated for two reasons: nonlinear nature of the switching node capacitances, and multi-resonant responses, especially in Interval II. An approximate, design-oriented analytical approach is developed in this section to arrive at relatively simple, yet accurate design guidelines for selection of the magnetizing inductance L_M and the secondary-side dead time t_{ds}.

Two approximations are applied in order to simplify the equivalent circuits in Fig. 5:

- The primary-side switching-node voltage v_P is approximated by a stair-step waveform during Interval II, as shown in Fig. 8. The approximation is justified by the fact that Interval II is relatively short compared to the overall ZVS transition time, and details of $nv_P(t)$ transitioning from 0 to V have little impact on the secondary-side ZVS transition waveforms. Furthermore, the approximate stair-
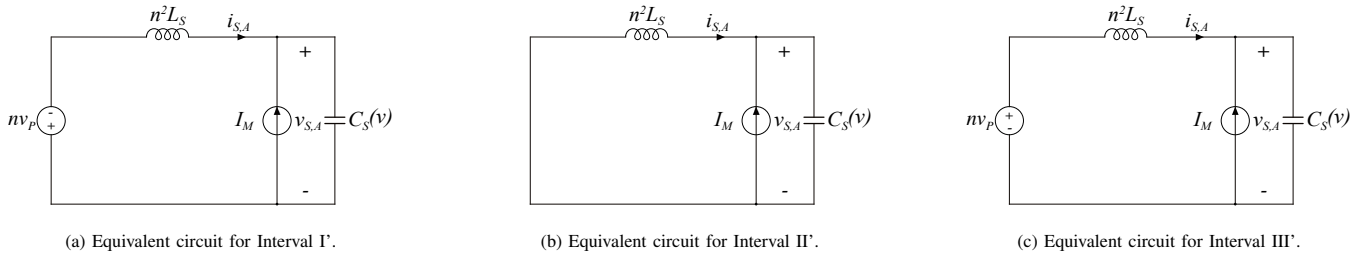
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(a) Equivalent circuit for Interval I'.   (b) Equivalent circuit for Interval II'.   (c) Equivalent circuit for Interval III'.

Fig. 7: Approximate equivalent circuits during ZVS transition.

Table IV:
Time instants of the approximated switching sequence

T'_1	$0.5(t_{ds} - 0.5t_{dp})$
T'_2	$0.5(t_{ds} + 0.5t_{dp})$
T'_3	t_{ds}

Table V:
Time intervals of the approximated switching sequence

Interval I'	$0 \le t < T'_1$
Interval II'	$T'_1 \le t < T'_2$
Interval III'	$T'_2 \le t < T'_3$

step waveform is symmetric around the mid-point of the transition, which simplifies the analysis.

- The magnetizing inductance current is considered constant and equal to I_M during the ZVS transition. This is justified by the fact that the magnetizing inductance is much larger than the series inductance, so that variations in i_M are relatively small during the ZVS transition.

The approximate equivalent circuits of the ZVS switching sequence are shown in Fig. 7. Definitions of the time instants and time intervals corresponding to the approximate switching sequence are given in Tables IV and V. The approximations greatly reduce complexity of the analysis, simplifying the switching sequence states to second-order circuits well suited for state-plane analysis. Since the switching sequence and the waveforms are symmetrical around $T_3/2$, as shown in Fig. 4, it is sufficient to perform the analysis over one half of the ZVS transition, from 0 to $T_3/2$.

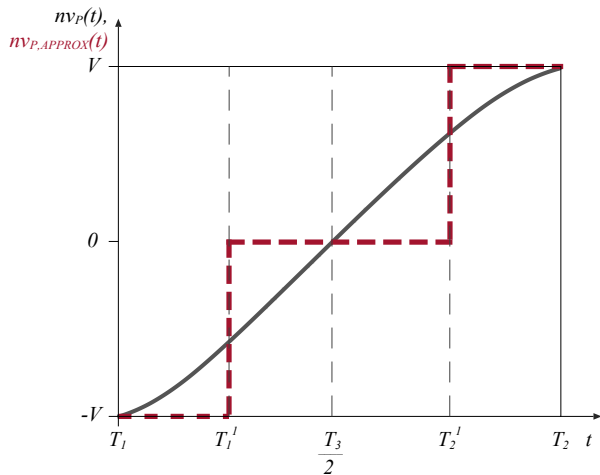In order to achieve ZVS with a minimum magnetizing current, $i_{S,A} + i_{M,A}$ should drop to zero at $T_3/2$, as discussed in Section II. Equivalently, $i_{S,A}$ should drop to $-I_M$. From the approximate model in Fig. 8, it can be seen that the primary-side voltage becomes zero at T'_1. Therefore, in order to keep $i_{S,A}$ constant and equal to $-I_M$, the secondary side switching node must drop to zero at T'_1 as well. Following this sequence of events, the entire half-transition is described by the circuit shown in Fig. 7(a), which further simplifies the analysis.

For state-plane analysis of the circuit in Fig. 7(a), a standard normalization is applied using the base values $V_{base} = V$ and $I_{base} = \frac{V_{base}}{R_0}$, where $R_0 = n\sqrt{\frac{L_S}{C_{S,EH}}}$. Since the analysis involves only one half of the ZVS transition, $C_{S,EH}$ is obtained by integrating the nonlinear $C_{S,hb}(v)$ curve up to one half of the full dc link voltage V, as shown in (6). The normalized voltage and current can be written as $m_{S,A} = \frac{v_{S,A}}{V_{base}}$ and $j_{S,A} = \frac{i_{S,A}}{I_{base}}$.

Fig. 9 illustrates the state-plane trajectory during Interval I'. In order for the normalized voltage to reach zero while the normalized current drops to $-J_M$, the following condition must be met

$$J_M = 1. \qquad (10)$$

Denormalizing (10), the required amplitude of the magnetizing current can be found as

$$I_M = \frac{V}{n}\sqrt{\frac{C_{S,EH}}{L_S}} = 2\sqrt{\frac{\pi f_{sw} C_{S,EH} P}{3\varphi_m(1 - \frac{\varphi_m}{\pi})}} \qquad (11)$$

and the required magnetizing inductance is

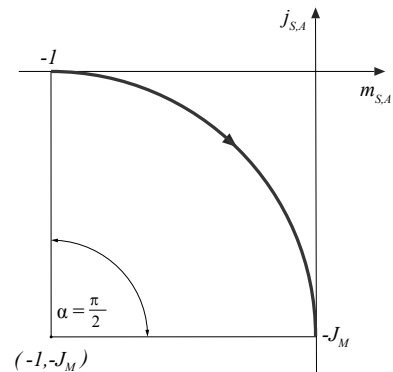$$L_M = \frac{V}{4I_M}\left(\frac{1}{f_{sw}} - t_{ds} - t_{dp}\right) \qquad (12)$$

Fig. 8: Exact and approximate waveforms of the primary side switching-node voltage $nv_p(t)$ during Interval II.

Fig. 9: State plane trajectory during interval I'.

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where t_{dp} can be found from (9). It remains to determine the secondary-side dead time t_{ds}.

Since the energy stored in the magnetizing inductance is just enough to discharge the switching node capacitance, the charge equivalent linear capacitance cannot be used to determine the secondary-side dead time. The rise time of the secondary side switching node can be estimated more accurately by solving the circuit in Fig. 7(a)

$$t_{ds} = \frac{t_{dp}}{2} + 2 \int_0^{\frac{V}{2}} \frac{C_{S,hb}(v)dv}{\sqrt{I_M^2 - \frac{4}{n^2 L_s} \int_0^v C_{S,hb}(v_x)v_x dv_x}}. \quad (13)$$

This result for the secondary dead time is accurate, and can be used to properly set the dead time in a practical implementation. With the goal of arriving at a simpler, closed-form solution for the required magnetizing inductance, it should be noted that the impact of t_{ds} in (12) is relatively small. An approximate expression for t_{ds} can be found from state-plane analysis illustrated in Fig. 9 by noting that T_1' interval corresponds to angle $\alpha = \pi/2$

$$\alpha = \frac{T_1'}{n\sqrt{L_S C_{S,EH}}} = \frac{\pi}{2}, \quad (14)$$

using the energy-equivalent secondary-side capacitance $C_{S,EH}$ evaluated over one half of the dc link voltage. Given that $T_1' = 0.5(t_{ds} - 0.5t_{dp})$, (14) yields an approximate expression for the secondary-side dead time

$$t_{ds,approx} = \frac{t_{dp}}{2} + \pi n \sqrt{L_S C_{S,EH}} \quad (15)$$

where L_S and t_{dp} can be found from (1) and (9), respectively.

Finally, a closed-form expression for the required magnetizing inductance L_M follows from (12)

$$L_M \approx \frac{V}{4I_M} \left(\frac{1}{f_{sw}} - t_{ds,approx} - t_{dp} \right) \quad (16)$$

where, in terms of the circuit specifications and parameter values, t_{dp} can be found from (9), I_M from (11), and $t_{ds,approx}$ from (15).

IV. EXPERIMENTAL RESULTS

The experimental setup of the isolated dc-to-3-phase ac module, using 900 V SiC MOSFETs (Wolfspeed Cree C3M0030090K) is shown in Fig. 10. The parameters of the converter are given in Table VI.

Primary-side dead time is calculated from (9), while secondary-side dead time and the magnetizing inductance are calculated according to (13) and (16), respectively, and the results are summarized in Table VII.

Table VI: Experimental prototype parameters

P	V	n	f_{sw}	φ_m	$C_{P,Q}$	$C_{S,EH}$
4 kW	600 V	1	100 kHz	20°	408 pF	312 pF

Table VII: Design parameters

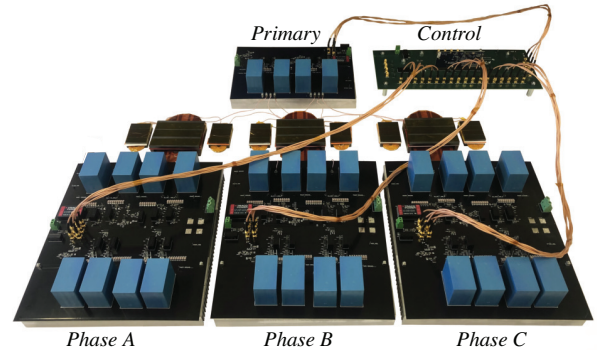| t_{dp}	t_{ds}	L_M
65 ns	548 ns	1.1 mH

Fig. 10: 600 V, 4 kW SiC-based experimental prototype.

Fig. 12 shows how the three-phase secondary QAB currents are summing up to a constant-envelope current on the primary side. The waveforms are shown for the currents $i_{S,A}$, $i_{S,B}$ and $i_{S,C}$ in Fig. 12(a), and the currents including the magnetizing currents in Fig. 12(b), which illustrate how the additional circulating currents are relatively small. Fig. 13(a) shows ZVS operation at the zero power crossing of phase A, while Fig. 13(b) confirms that the measured waveforms closely match the theoretical waveforms shown in Fig. 4.

In order to verify the approximations introduced in Section III-C, two model based simulations are performed, and compared with the experimental results. An accurate model is developed based on the equivalent circuits shown in Fig. 5. A simpler model, which is used to derive design equations in Section III, is based on the equivalent circuits shown in Fig. 7. Fig. 11 shows a good agreement between the state-plane trajectories obtained from the accurate model, from the approximate model, and from the experimental waveforms.

Measured efficiency of the prototype converter is shown in
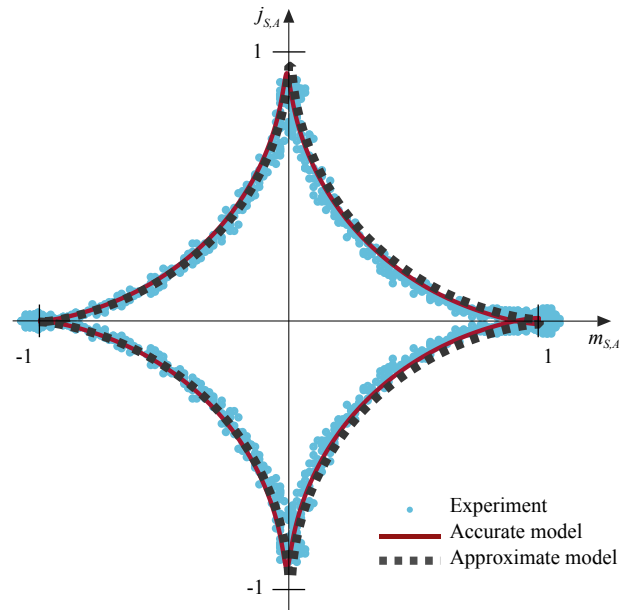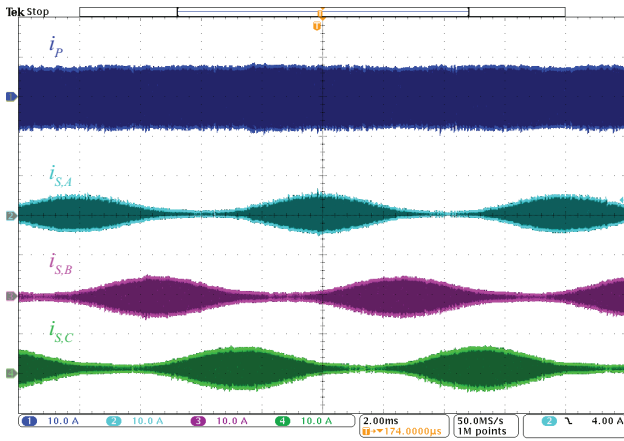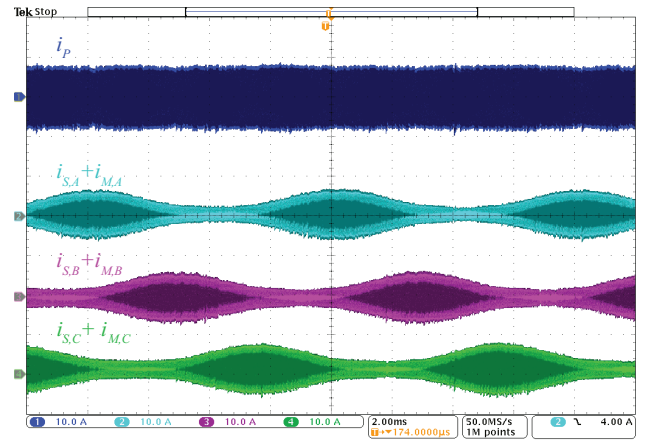

Fig. 11: State plane trajectory at the time Phase A power is zero. Experimental results are overlapped with solutions based on accurate and approximate models.
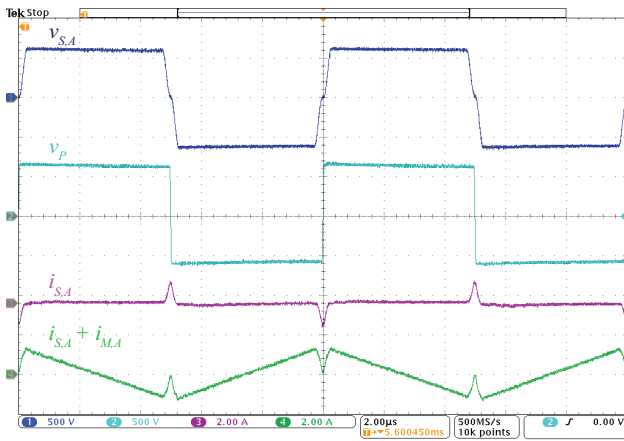
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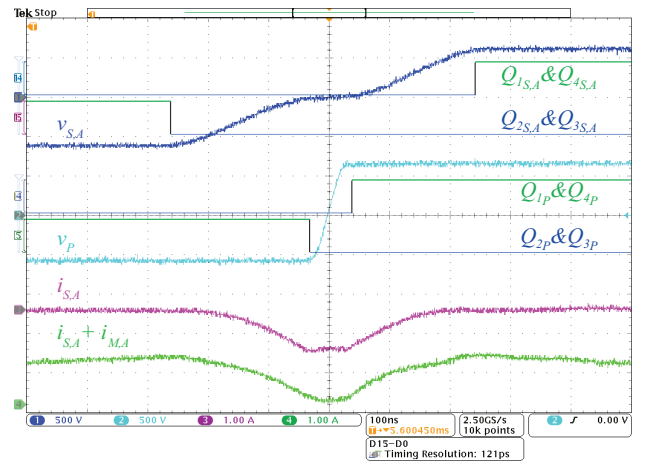(a) Primary current i_P, and secondary currents through L_s.

(b) Primary current i_P, and secondary currents through L_s and L_M.

Fig. 12: Quadruple active bridge primary and secondary currents.

(a) Switching-node voltages $v_{S,A}$, v_P, and currents $i_{S,A}$ and $i_{S,A} + i_{M,A}$.

(b) Waveforms during ZVS transition.

Fig. 13: Waveforms illustrating zero voltage switching at the zero power instant for phase A.

Fig. 14 as a function of the average output power. Efficiency remains greater than 98.5% from 1 kW to 4 kW, with a peak efficiency of 99.0%. In Fig. 15, measured efficiency is compared with efficiency of the conventionally operated prototype where all the circuit parameters are the same, but the transformer core does not include an air gap and the magnetizing inductance is much larger. The prototype with the optimized L_M and optimized dead times features a much flatter efficiency curve, and substantial efficiency improvements compared to the conventional design, especially at lower power levels. At the rated power (4 kW), measured efficiency of the conventionally operated prototype is 97.6%, while measured efficiency of the optimized prototype increases to 98.9%, which corresponds to an overall loss reduction by more than 50%.

V. CONCLUSIONS

This paper shows how the transformer magnetizing current can be used to achieve zero voltage switching (ZVS) throughout the line cycle in a transformer-isolated quadruple active bridge (QAB) dc-dc converter feeding three-phase ac output.
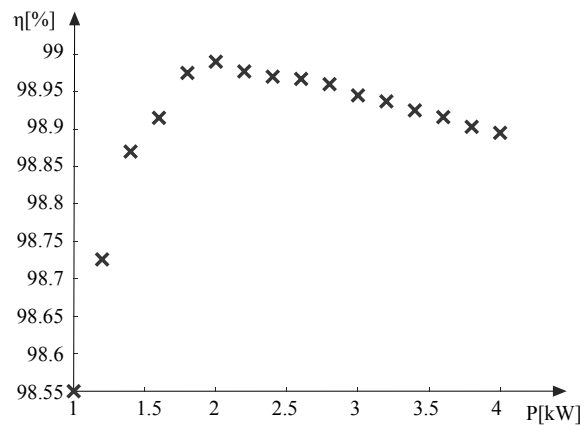

Fig. 14: Efficiency of the experimental prototype using the optimized magnetizing inductance and dead times.

By placing an airgap into the high frequency transformer's core, a circulating magnetizing current is introduced, which makes ZVS possible during low power transfer intervals.
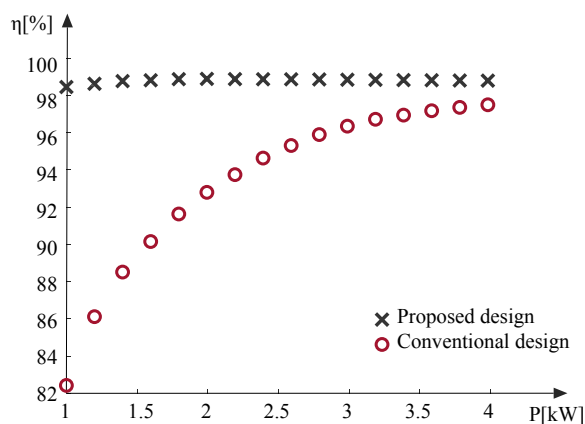
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Fig. 15: Measured efficiency of the conventionally operated prototype (with large magnetizing inductance), compared to the measured efficiency of the experimental prototype with optimized magnetizing inductance and dead times.

Simple phase shift modulation is employed, without the need for changing modes over the line cycle. A detailed analysis of the switching transient is presented, including effects of the nonlinear device capacitances. Suitable approximations are introduced to obtain closed form, design-oriented expressions for the magnetizing inductance, and the primary-side and secondary-side dead times, so that ZVS is achieved, while minimizing the magnetizing current, without loss of accuracy. The approach is particularly well suited for higher voltage applications, where hard switching losses can be significant. Experimental results on a SiC-based 600 V, 4 kW prototype operating at 100 kHz verify the model, and show that efficiency remains greater than 98.5% over 1-4 kW average output power, with 99.0% peak efficiency and more than 50% loss reduction at rated power compared to conventionally operated prototype. Efficiency improvements are even higher at lower power levels.

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