Photovoltaic AC Module Composed of a Very Large Number of Interleaved Inverters

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Abstract—**A photovoltaic panel fitted with a large collection of low-power inverters integrated at the level of individual solar cells is used to design an ac module. To facilitate dc-ac power conversion, the inverter aggregate is controlled using interleaved carrier pulse width modulation. Every solar cell operates at its maximum power point even when the photovoltaic panel is partially shaded. Additionally, a very low switching frequency can be used to minimize switching losses without increasing output distortion. Both system-level and local control strategies are developed to regulate power output, energy storage, and ensure stable operation. Experimental and simulation results are presented to verify and demonstrate the proposed method.**

I. INTRODUCTION

Photovoltaic (PV) system topologies have been moving from large centralized systems to low-power distributed systems such as microinverters. Recent interest has focused on developing a solar panel which directly interfaces to the ac grid without external dc wiring. This is referred to as a PVAC module [1]. This paper proposes that each PVAC module be fitted with a very large number of low-power inverters integrated at the individual solar cell level. The microinverter approach to ac module design has been to interface each panel to the grid through a single dedicated inverter. Although microinverter systems optimize performance by tracking the panel's maximum power point (MPP), mismatched power production among solar cells, due to partial shading on a particular panel, can severely degrade power output. It has been demonstrated that if a single cell on a 72-cell panel is shaded, the panel power output can diminish by more than 25% [2]. This strong dependence of overall power output on single cells suggests that the power-electronic conversion process should occur at the individual solar cell level. The proposed system, which is controlled using interleaved carrier pulse width modulation (ICPWM), optimizes individual cell performance, utilizes as low switching frequency, and achieves a low-distortion ac output current.

II. BACKGROUND

A $2n + 1$ level voltage source inverter may be constructed given a system with n H-bridges supplied by independent bus voltage sources by configuring the outputs of the H-bridges in series as shown in Fig. 1. Using a variation of established PWM techniques outlined in [3]–[5], each pair of carrier waveforms associated with a three-level H-bridge inverter is phase shifted by a unique multiple of T_c/n, where T_c is the period of the carrier waveform. One common modulation signal with period T_m is used. Low distortion is maintained even as the switching frequency is lowered as the number of interleaved inverters grows.

Figs. 2–4 summarize the behavior of an example system composed of five three-level H-bridge inverters. Fig. 2 shows the sample system interleaved carrier-pair waveforms and sine-wave modulation signal. The carrier frequency was chosen
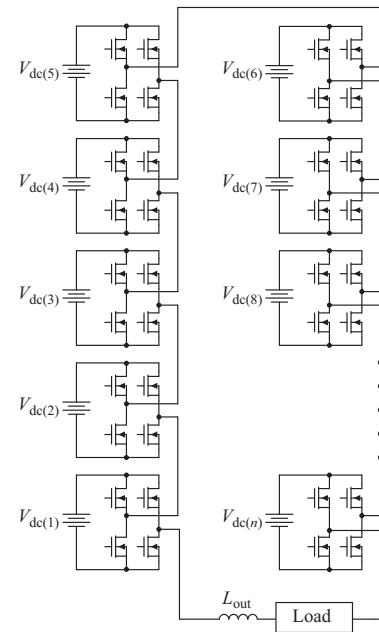

Figure 1. System topology of multi-level inverter composed of n cascaded single-phase H-bridges

such that $T_m = 3T_c$. Fig. 3 shows the resulting PWM comparator outputs corresponding to each pair of H-bridge legs. The output voltage of the individual H-bridges and the low-distortion ac voltage across the 5 series inverters can be seen in Fig. 4 . In general, output voltage waveform characteristics are dependent on the carrier waveform shape. A detailed analysis of carrier waveforms for multi-carrier PWM
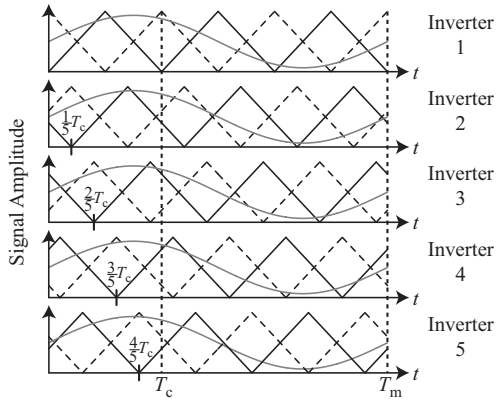
Figure 2. Interleaved carrier waveforms of 5 three-level inverters and common modulation signal
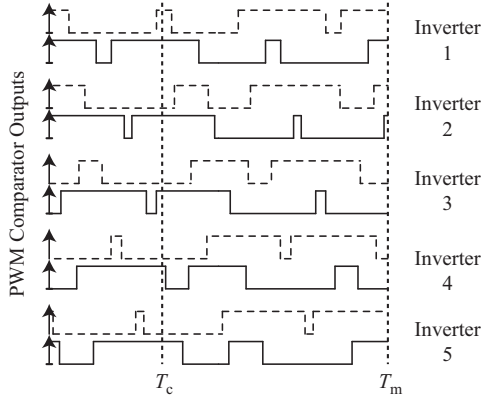

Figure 4. Voltage output of each H-bridge inverter and voltage across 5 series connected interleaved inverters

Figure 3. PWM comparator outputs used to produce 3-level PWM

Figure 5. Circuit topology of ac module comprised of n series connected interleaved inverters

can be found in [6].

Typically, multi-level inverters aim at five or seven levels because of perceived complexity with higher levels [7], [8]. However, extreme inverter counts with interleaving offer major benefits such as cancellation of many high-frequency terms [5]. The proposed system allows for a low switching frequency and a low voltage rating. The output filter inductance, L_{out}, can be reduced dramatically in comparison to a single 3-level inverter while achieving lower output current distortion. The distributed architecture inherent to a solar panel allows the ICPWM technique to be applied.

III. AC MODULE COMPRISED OF INTERLEAVED CONVERTERS

The proposed system, as shown in Fig. 5, consists of n individual solar cells (or groups of cells) connected to a dedicated sub-inverter. Each sub-inverter consists of a boost converter, an energy storage device supporting its local bus voltage, and an H-bridge controlled by ICPWM. A typical PV module consisting of 72 solar cells may be used to create an ac module composed of 72 series-connected sub-inverters. Common modulation and interleaving produces system performance which mimics the behavior of a $2 \times 72 + 1$ level inverter. Considering the modest power rating of each sub-inverter
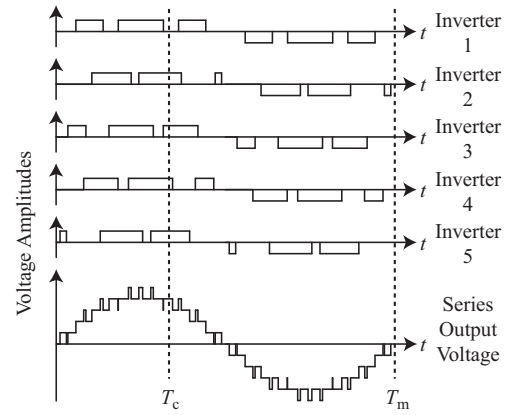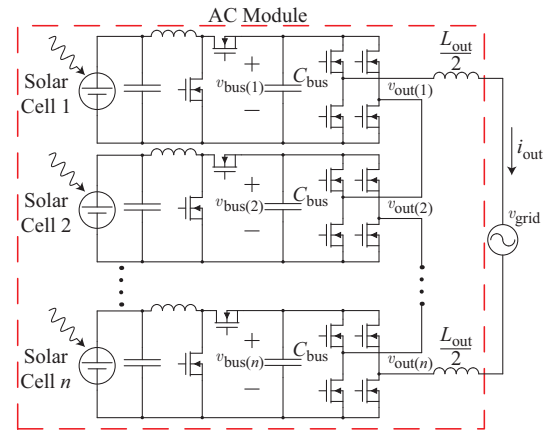
(~ 5 W), the power semiconductor devices and control circuitry of each sub-inverter may be fully or partially combined into an integrated circuit. As cell level maximum power point trackers (MPPT) are utilized, harvested energy is maximized despite partial shading conditions.

The system of n sub-inverters is managed using one master current controller and n local output bridge controllers, as shown in Fig. 6. Using output current, grid voltage, and bus voltage measurements, the master current controller creates a system modulation signal, M_{sys}, such that total output power is regulated. M_{sys}, is scaled by each local output bridge controller so that local stored energy in each sub-inverter is controlled. The boost converter associated with each sub-inverter operates independently and functions solely to track the cell maximum output power.

The master current controller, as shown in Fig. 7, is designed to maintain system-level energy balance: in a single-phase grid-connected inverter application, double frequency power is delivered to the grid while total energy stored in the bus capacitors must be held nearly constant. The sum of the squared capacitor voltages is used to estimate the total available PV power. Using energy conservation and neglecting

Figure 6.   Control topology of interleaved inverter system

Figure 7.   Master current controller

circuit losses, the approximated PV power, P_{net}, is

$$\sum_{k=1}^{n} i_{cell(k)} v_{cell(k)} \approx P_{net} = i_{out} v_{grid} + \frac{d}{dt} \frac{1}{2} C_{bus} \sum_{k=1}^{n} v_{bus(k)}^2 \quad (1)$$

Because the derivative calculation in (1) can be problematic, the derivative may be approximated using a lead compensator with the transfer function

$$G_{deriv}(s) = \frac{s}{\tau_{deriv} s + 1} \quad (2)$$

The value $\sqrt{2} P_{net} / V_{LLrms}$, denoted as i_{approx} in Fig. 7, is the dominant term in the current command magnitude i_{pk}^*. A bus voltage PI controller can generate a small adjustment term, i_{adj}, such that the sum of the capacitor voltages neither collapses nor increases without bounds because of small errors between the actual and desired output power. The bus capacitor voltage sum must be maintained such that it always exceeds the instantaneous grid voltage. In 240 V grid-connected applications, a reasonable capacitor voltage sum command, V_{sysbus}^*, is 400 V. A phase-locked loop generates a factor equal to $\sin(\omega_s t + \phi)$,

such that the ac current command, i^*, has a frequency equal to v_{grid}. The phase shift, ϕ, of the current command relative to the grid voltage can be used to control the amount of reactive power delivered to the grid. If $\phi = 0$, only real power is generated. The measured current, i_{out}, is then compared to i^* to create the system modulation signal M_{sys}.

Figure 8.   Output bridge controller of kth sub-inverter

The output bridge controller of the kth sub-inverter using ICPWM is shown in Fig. 8. Its primary purpose is to regulate local energy balance by scaling M_{sys} such that the voltage across an individual bus capacitor remains within desired bounds. In Fig. 8, a reasonable value for the capacitor voltage command, V_{bus}^*, is $(400 \text{ V})/n$. The cutoff frequency of the bus voltage measurement low-pass filter must be sufficiently lower than the voltage ripple double-frequency. The capacitor voltage PI controller output is multiplied by M_{sys} to create a scaled modulation signal, $M_{(k)}$. The interleaved carrier-pair of the kth sub-inverter are connected to a pair of comparators to generate the output bridge gate signals. Using the proposed local controller, sub-inverters which correspond to shaded PV cells will have a reduced modulation amplitude such that the voltage ripple across the local bus is reduced and power delivered to the grid by the sub-inverter is in short bursts. The proposed master and local controller parameters are summarized in Table I.

TABLE I
PARAMETERS OF MASTER AND LOCAL CONTROLLERS

$K_{psysbus} = 0.00375$	$K_{isysbus} = 0.1$	$\tau_{vsysbus} = \frac{1}{2\pi 10}$
$\tau_{deriv} = \frac{1}{2\pi 10^5}$	$K_p = \frac{10}{22.1}$	$K_i = \frac{10^6}{22.1 \times 8.2}$
$K_{pbus} = 200 K_{psysbus}$	$K_{ibus} = 10 K_{isysbus}$	$\tau_{vbus} = \frac{1}{2\pi 5}$

SIMULATION RESULTS

Simulation results were prepared for a grid-connected 250 W ac module consisting of 72 sub-inverters. Each sub-inverter bus contained a 5 mF energy storage capacitor. A total output filter inductance of 500 μH was used. The 72 H-bridge

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carrier-pairs were selected such that each 300 Hz sawtooth carrier pair corresponding to an H-bridge was phase-shifted by a unique multiple of $1/(72{\times}300)$ s. Simulation results are presented to illustrate system performance both during uniform insolation and partial shading.

A. Uniform Insolation

The simulation results in Figs. 9–10 summarize the expected system behavior when all sub-inverters are producing equal average power and the average aggregate power output is 250 W. As shown in Fig. 9, the current and voltage waveforms produced by the large number of interleaved converters have low distortion and rated double-frequency power is delivered to the grid. To illustrate the behavior of one sub-inverter, Fig. 10 shows the voltage across the 30th sub-inverter and its power output. Simulation results confirm stable operation at both the local and system level.
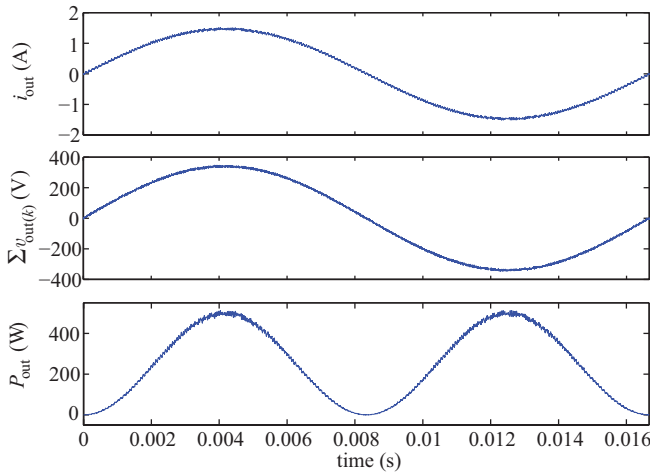
Figure 9. AC module performance during uniform insolation: (Top) System output current with THD of 1.77%; (Middle) Output voltage across all series sub-inverters; (Bottom) Double-frequency power delivered to grid
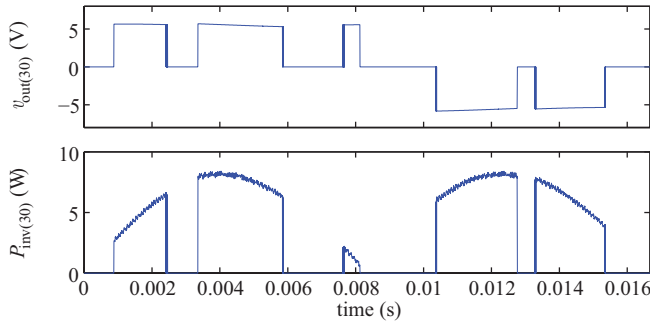
Figure 10. Voltage and power output of one sub-inverter: (Top) Voltage output of 30th sub-inverter H-bridge with 300 Hz switching frequency; (Bottom) Power produced by 30th sub-inverter

B. Non-Uniform Insolation: Partial Shading

The proposed system and its accompanying control generally can accommodate non-uniform average power production by solar cells and their corresponding sub-inverters.

The following simulation results illustrate system performance during extreme partial shading conditions when 10 of the 72 solar cells are shaded. Specifically, the power production of the shaded cells was reduced by 90% in comparison to the unshaded cells which each produced the average rated power of 250/72 W. Fig. 11 shows that the system maintains low distortion current and voltage output despite shading. Although total delivered power is reduced, it should be noted that unlike conventional systems, the shaded cells do not disproportionately reduce power output because cell level MPPT is employed.
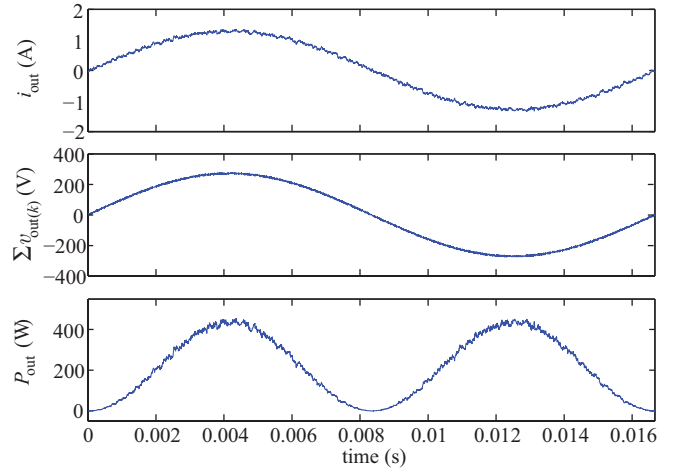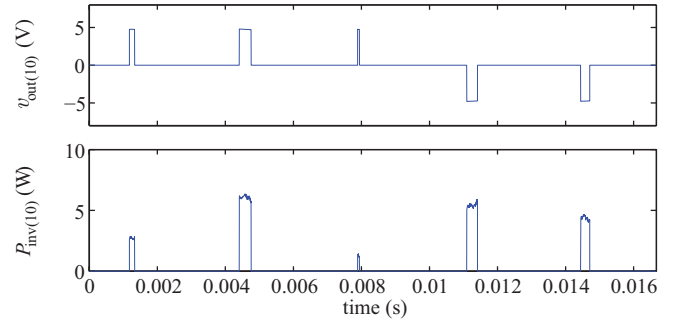

Figure 11. AC module performance during partial shading: (Top) System output current with THD of 3.37%; (Middle) Output voltage across all series sub-inverters; (Bottom) Double-frequency power delivered to grid

Figure 12. Voltage and power output of sub-inverter corresponding to shaded cell: (Top) Voltage output of 10th sub-inverter H-bridge with 300 Hz switching frequency; (Bottom) Reduced power produced by 10th sub-inverter

Sub-inverters with shaded cells will have a reduced modulation signal amplitude as each sub-inverter uses the local controller shown in Fig. 8. As a result, these sub-inverters will have a reduced average power output and local bus capacitor charge depletion will be prevented. To illustrate the performance of one sub-inverter corresponding to a shaded cell, Fig. 12 shows the output voltage and power produced by the 10th sub-inverter. It can be seen that a sub-inverter with a shaded cell will deliver power in brief bursts. The sub-inverters

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which correspond to unshaded cells have voltage and power waveforms similar to that shown in Fig. 10.
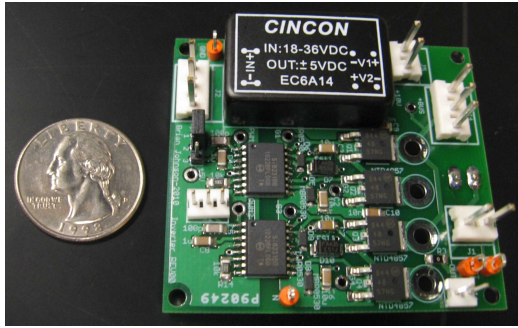
EXPERIMENTAL RESULTS

Figure 13.   One H-bridge inverter

A 16×2+1 level inverter composed of 16 series-connected three-level H-bridges was tested experimentally. Each H-bridge inverter, as shown in Fig. 13, contains an independent and isolated 5 V dc bus. The inverter composed of 16 H-bridges supplied a $100\Omega + 300\mu H$ RL load with a 60 Hz ac voltage with an 80 V amplitude. The system has the topology shown in Fig. 1. Each H-bridge utilized a pair of 180 Hz sawtooth carriers that were phase-shifted by a unique multiple of 1/(16×180) s and a common 60 Hz modulation signal was used. The modulation signal was created using an analog signal generator while the interleaved carriers, comparators, and gate logic signals were implemented by an FPGA. Fig. 14 contains the system modulation signal and the resulting PWM comparator outputs corresponding to one leg of each H-bridge. Fig. 15 shows the voltage across one three-level H-bridge inverter, the total voltage across the 16 series H-bridges, and the load current.
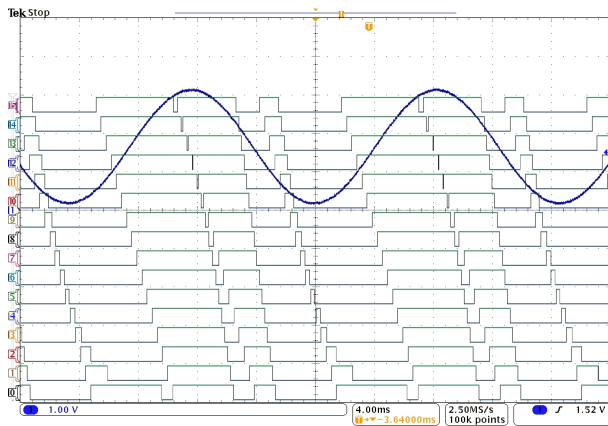

Figure 14.   60 Hz modulation signal and PWM comparator outputs of 16 interleaved inverters

IV. CONCLUSION AND FUTURE WORK

An ac module consisting of interleaved low-power solar cell inverters was presented utilizing the distributed architecture
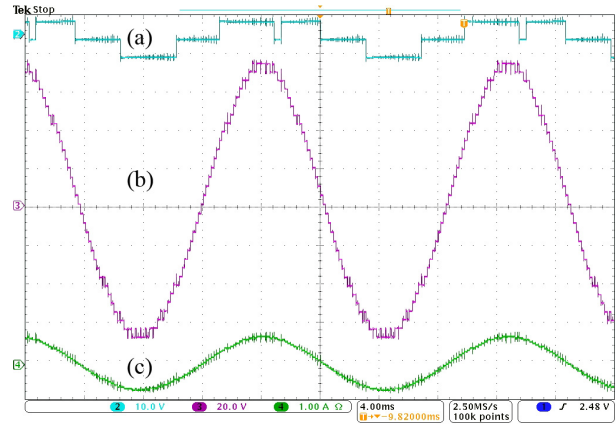

Figure 15.   Experimental results based on 180 Hz switching of 16 series inverters: (a) Voltage across a single H-bridge; (b) Voltage across 16 series-connected interleaved inverters; (c) Load current

inherent to a PV panel. A control system for managing both system and local energy while maximizing system level power output was demonstrated. Using ICPWM, a low-distortion output current was achieved using a relatively low switching frequency and a small output filter inductance. Simulation results illustrated operation of an ac module comprised of 72 interleaved inverters and experimental results verified multi-level inverter operation. Further work will be aimed at eliminating the need for a master controller such that all sub-inverters will operate autonomously. An AC module for experimentation is also under development.

REFERENCES

[1] S. Kjaer, J. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1292 – 1306, 2005.

[2] W. Xiao, N. Ozog, and W. Dunford, "Topology study of photovoltaic interface for maximum power point tracking," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 3, pp. 1696 –1704, 2007.

[3] J. Kimball and M. Zawodniok, "Reducing common-mode voltage in three-phase sine-triangle PWM with interleaved carriers," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1508 –1513, 2010.

[4] B. McGrath and D. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 49, pp. 858 – 867, Aug. 2002.

[5] D. Holmes and T. Lipo, *Pulse Width Modulation for Power Converters*. Piscataway, NJ: IEEE Press, 2003.

[6] P. Krein, R. Balog, and X. Geng, "High-frequency link inverter for fuel cells based on multiple-carrier PWM," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1279 – 1288, 2004.

[7] G. Mondal, K. Gopakumar, P. Tekwani, and E. Levi, "A reduced-switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2344 –2351, 2007.

[8] O. Lopez, J. Alvarez, J. Doval-Gandoy, and F. Freijedo, "Multilevel multiphase space vector PWM algorithm," *IEEE Transactions on Industrial Electronics*, vol. 55, pp. 1933 –1942, May 2008.