Modeling and Simulation of Power-electronic Inverters in Analog Electronic Circuit Simulators

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***Abstract*—This paper demonstrates how equivalent-circuit representations of grid-following power-electronic inverters can be realized within a SPICE-based development environment using common circuit components and VerilogA code. This facilitates computationally lean simulations of inverter networks leveraging the strengths of SPICE in large-scale simulations. We validate the approach with time-domain simulations for a modified version of the IEEE standard 118-bus system modeled in Virtuoso (a SPICE-based solver). Simulation results are compared—focusing on accuracy and computation speed—with results from a commonly used power-electronics simulation package. We note a significant decrease in simulation time with comparable signal resolution when simulating the network in SPICE.**

I. Introduction

Renewable energy resources (such as photovoltaic arrays and wind turbines), electric vehicles, and energy-storage devices interface with the bulk power grid primarily through grid-following inverters: power-electronic circuits with switching semiconductor devices that have complex physical dynamics and involved (typically digital) controllers [1]–[4]. Due to the nonlinear nature of the involved dynamics and the complexity induced by their networked interactions in distribution and transmission systems, computationally efficient and accurate means to model and simulate networks of inverter-interfaced resources continue to receive interest [5].

This paper contributes to a recently proposed equivalent-circuit modeling approach that yields integrated and unified models for inverters cutting across their physical- and control-layer dynamics [6], [7]. Equivalent-circuit models can be realized using common circuit elements available in electronics simulation software, and thereby hold the promise to facilitate simulations for large networks compared to conventional modeling approaches that demarcate physical- and control-layer dynamics. In this paper, we explore simulating equivalent-circuit inverter models within popular circuit simulators such as SPICE [8]. It is quite nonstandard to pursue *system-level* simulation (network dynamics as well as inverter control- and physical-layer dynamics) in circuit simulator software such as SPICE. Such simulations are typically performed with software such as PLECS [9] and PSCAD [10]. That said, it is quite common to pursue modeling and simulation of power-electronics *components* and *circuits* with electronic circuit simulators [11], [12]. For instance, SPICE is used for modeling non-idealized switching dynamics in power electronics circuits such as soft-switching current source inverters or switched-capacitor DC-DC converters [13], [14]. While SPICE (and SPICE-type software) is proficient at simulating circuit- and component-level dynamics in high detail, such software packages often do not include models for components and controllers that are critical to represent power-electronics circuits in larger networks. The effort required to create and maintain such models would be substantial. Using equivalent-circuit models for *all* constituent elements (control+physical) in power-electronics paves the way to network-level simulations with circuit simulators.

Overcoming the deficiency of component- and controller-level modeling by leveraging circuit-based representations facilitates large-scale power networks to be realized in software like Cadence Virtuoso Layout Suite. Typically used for VLSI design, Cadence Virtuoso is a powerful layout tool that offers the ability to script the construction of electrical networks. Virtuoso utilizes Cadence Spectre, a SPICE-based simulator, to simulate large electrical networks. The main challenge involved is representing filter dynamics, dynamics of phase-locked loops, controllers, and reference transformations in this simulation environment. This work address the issues that arise when porting over such power-electronics subsystem models into a SPICE-based environment.

The remainder of this paper is organized as follows. In Section II, we overview the averaged dynamics of the inverter and the equivalent-circuit representation for all subsystems. Alongside this, we outline methods to realize the inverter model within the Cadence Virtuoso Layout Suite using standard circuit libraries and VerilogA code blocks. Numerical simulations for a modified IEEE 118-bus network with 54 inverters are provided in Section III; they establish the accuracy and computational benefits of the SPICE-based simulator approach. We conclude the paper in Section IV with a few directions for future work.

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II. SPICE Representations: Inverter & Network

Figure 1(a) illustrates the topology of the three-phase grid-following inverter we examine in this work. This is a standard and prototypical example, and is widely studied in the literature [1]. The inverter is voltage sourced with an LC output filter, and the control architecture includes a current controller, phase-locked loop, and reference frame transformations that facilitate control. For a single inverter, the connection to the bulk grid is modeled as an infinite bus of fixed frequency ω_{g}, phase angle θ_{g}, and voltage magnitude, E. The equivalent-circuit representation of the averaged dynamics (Fig. 1(b)) consists solely of common circuit elements [6], [7]. We discuss (individually) next, the control- and physical-layer subsystems focusing on their SPICE implementations.

A. Current Controller

The current controller (CC) includes proportional-integral (PI) compensators with gains of $k^{\mathrm{p}}_{\mathrm{CC}}$, $k^{\mathrm{i}}_{\mathrm{CC}}$, and feedforward terms $\omega L_{\mathrm{f}} i_{\mathrm{q}}$, $\omega L_{\mathrm{f}} i_{\mathrm{d}}$, to compensate for the output filter dynamics. The compensators generate voltage reference outputs $v^{\mathrm{t}}_{\mathrm{d}}$, $v^{\mathrm{t}}_{\mathrm{q}}$. The PI controllers for the current loop operate on reference current-source inputs, $i^{\star}_{\mathrm{d}}$ or $i^{\star}_{\mathrm{q}}$ that correspond to desired inverter active- and reactive-power outputs.

The integrating and proportional terms of the PI controllers are represented as RC circuits with capacitance $1/k^{\mathrm{i}}_{\mathrm{CC}}$ and resistance $k^{\mathrm{p}}_{\mathrm{CC}}$ for the equivalent-circuit model. These components are directly translated into Virtuoso as ideal resistors and capacitors with programmable values. The remaining feedforward term of the PI controller is shown as a dependent voltage source of value $v_{\mathrm{d}} - \omega L_{\mathrm{f}} i_{\mathrm{q}}$ for the d axis and $v_{\mathrm{q}} + \omega L_{\mathrm{f}} i_{\mathrm{d}}$ for the q axis. These are modeled using the voltage controlled voltage source (VCVS) in Virtuoso.

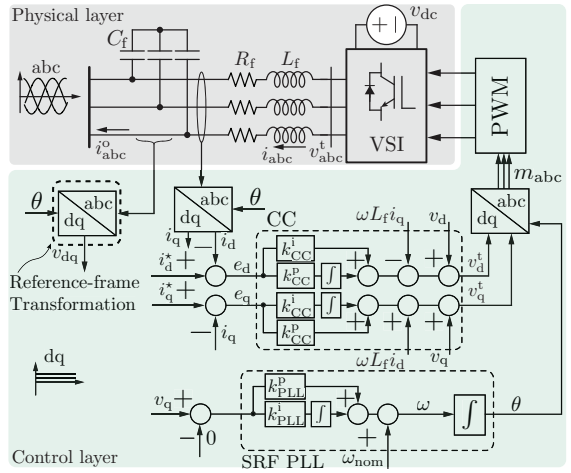
B. Reference Frame Transformations

Analysis and control implementation for the inverters as well as the description of the electrical-network dynamics are all presented in appropriately defined direct-quadrate reference frames. For an individual inverter, the controllers operate with respect to a local dq reference frame based on the angle generated from the phase-locked loop, θ. On the other hand, network-level signals are represented with respect to a global DQ reference frame at angle θ_{g} (which is the phase angle corresponding to the infinite bus). Defining $\delta := \theta - \theta_{\mathrm{g}}$, we obtain the following transformation for voltages expressed in the global DQ and local dq reference frames:

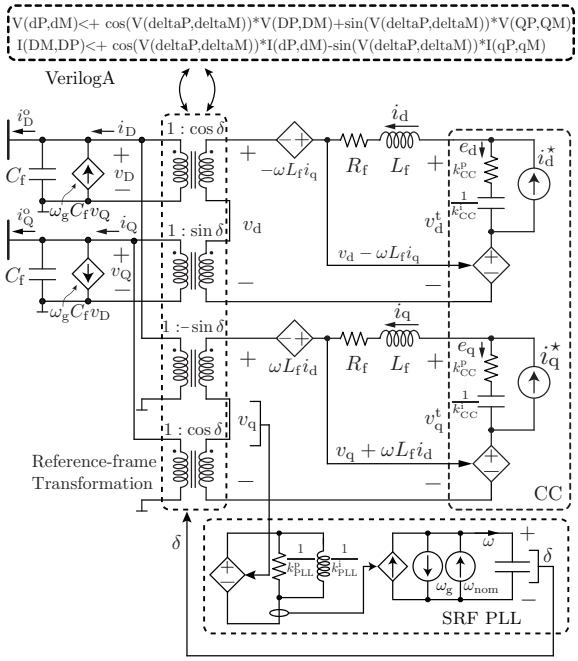
$$\begin{bmatrix} v_{\mathrm{d}} \\ v_{\mathrm{q}} \end{bmatrix} = \begin{bmatrix} \cos\delta & \sin\delta \\ -\sin\delta & \cos\delta \end{bmatrix} \begin{bmatrix} v_{\mathrm{D}} \\ v_{\mathrm{Q}} \end{bmatrix}. \tag{1}$$

Similar expressions follow for currents and they are not repeated. This system of non-linear equations that relates the two reference frames is represented with ideal transformers within the equivalent-circuit model (see Fig. 1(b)). Note that each transformer operates on DC signals and has a variable turns ratio that is a nonlinear function of angle δ.

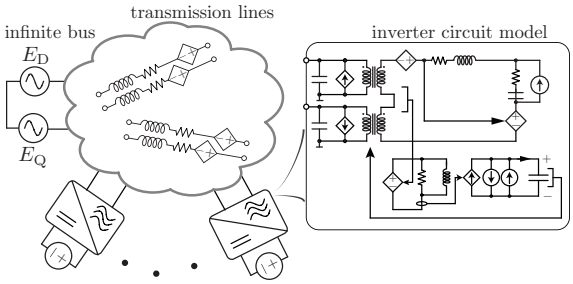
A limitation of the ideal transformer model in Virtuoso is that the model does not allow for time dependent turn ratios.



(a) switched model of inverter



(b) equivalent circuit model of inverter



(c) equivalent circuit model of network

Fig. 1. (a) Detailed switched model for grid-following inverter; (b) Corresponding equivalent-circuit model; (c) Network with inverters, transmission lines, and an infinite bus modeling an aggregated representation of the bulk power grid. Notably, the entire network in (c) is composed of circuit elements.

To circumvent this, a custom block composed of VerilogA code is created to perform the function of the variable turn transformers. The transformation (1) and the corresponding expression for current are then expressed in VerilogA as:

```
V(dP,dM)<+ cos(V(deltaP,deltaM))*V(DP,DM)
        +sin(V(deltaP,deltaM))*V(QP,QM)
I(DM,DP)<+ cos(V(deltaP,deltaM))*I(dP,dM)
        -sin(V(deltaP,deltaM))*I(qP,qM)
```

where V(deltaP, deltaM) is the voltage across the unit capacitance with voltage δ in Fig. 1(b). In VerilogA syntax, the voltage difference from node 1 to node 2 is written as $V(node1, node2)$, while the current through node 1 in the direction of node 2 is written as $I(node1, node2)$. The VerilogA code is turned into a symbol and can be placed within a Virtuoso schematic like any other element.

C. Phase-locked Loop

The synchronous reference frame (SRF) phase-locked loop (PLL) tracks the phase-a angle of the inverter terminal voltage. The PLL partly consists of a PI controller with integral gain of $k^{\mathrm{i}}_{\mathrm{PLL}}$ and proportional gain of $k^{\mathrm{p}}_{\mathrm{PLL}}$. As shown in Fig. 1(b), the equivalent circuit is a parallel combination of a dependent voltage source, a resistor $1/k^{\mathrm{p}}_{\mathrm{PLL}}$, and an inductor $1/k^{\mathrm{i}}_{\mathrm{PLL}}$.

For the Virtuoso implementation, the dependent voltage source is modeled using a unity-gain VCVS that taps the top and bottom voltages of the v_{q} ideal transformers for its input. An ideal resistor and inductor of programmable values are placed in parallel with the VCVS. The model for the equivalent-circuit PLL outputs the angle δ as the voltage across a unit-value capacitor which is driven by three parallel current sources. The first current source is dependent on the total current flowing through the PI controller loop. This dependent current source is realized in Virtuoso using the current controlled current source (CCCS) in the Virtuoso analog library. The CCCS requires a $0[\mathrm{V}]$ DC voltage source to be placed in series with the branch that will have its current measured. This acts as an ammeter and relays the current value to the CCCS. The two other current sources present are modeled as DC current sources with values of ω_{g} and ω_{nom}.

D. LC Output Filter

The LC output filter of the inverter is modeled with inductor dynamics represented in the local dq frame and the capacitor dynamics in the global DQ frame. This is for analytical and notational convenience. In the equivalent-circuit model of the inverter, this manifests as the filter inductor, L_{f} with R_{f}, being located on the secondary-side of the transformers, and therefore, in the local dq frame. The Virtuoso implementation involves an ideal resistor and inductor of programmable values. The filter capacitance, C_{f} is placed on the primary-side of the transformers to be within the global DQ frame. The dynamics of the filter discussed above are given by:

$$\begin{bmatrix}\dot{i}_{\mathrm{d}}\\ \dot{i}_{\mathrm{q}}\end{bmatrix} = \begin{bmatrix}\frac{-R_{\mathrm{f}}}{L_{\mathrm{f}}} & \omega\\ -\omega & \frac{-R_{\mathrm{f}}}{L_{\mathrm{f}}}\end{bmatrix}\begin{bmatrix}i_{\mathrm{d}}\\ i_{\mathrm{q}}\end{bmatrix} + \frac{1}{L_{\mathrm{f}}}\begin{bmatrix}v_{\mathrm{d}}-v^{\mathrm{t}}_{\mathrm{d}}\\ v_{\mathrm{q}}-v^{\mathrm{t}}_{\mathrm{q}}\end{bmatrix}, \qquad (2)$$

$$\begin{bmatrix}\dot{v}_{\mathrm{D}}\\ \dot{v}_{\mathrm{Q}}\end{bmatrix} = \begin{bmatrix}0 & \omega_{\mathrm{g}}\\ -\omega_{\mathrm{g}} & 0\end{bmatrix}\begin{bmatrix}v_{\mathrm{D}}\\ v_{\mathrm{Q}}\end{bmatrix} + \frac{1}{C_{\mathrm{f}}}\begin{bmatrix}i_{\mathrm{D}}-i^{\mathrm{o}}_{\mathrm{D}}\\ i_{\mathrm{Q}}-i^{\mathrm{o}}_{\mathrm{Q}}\end{bmatrix}, \qquad (3)$$

where $(v^{\mathrm{t}}_{\mathrm{d}}, v^{\mathrm{t}}_{\mathrm{q}})$ is the voltage at the inverter switched terminals in the local dq frame and $(i^{\mathrm{o}}_{\mathrm{D}}, i^{\mathrm{o}}_{\mathrm{Q}})$ is the current injection into the network in the global DQ frame. To model the off-diagonal terms of the system matrices in (2)–(3), the equivalent-circuit inverter model includes a dependent current source in parallel with the filter capacitor and a dependent voltage source in series with the filter inductor, as shown in Fig. 1(b). For the D-axis, the dependent voltage source in series with the filter inductor outputs the negative product of L_{f} and currents ω and i_{q}. To model this in Virtuoso, the same method of using a 0 [V] DC voltage source as an ammeter for the branches that contain ω, in the PLL, and i_{q}, in the Q-axis side, is used. In order to take the product of these two values, a polynomial current controlled voltage source (PCCVS) from the analog library of Virtuoso is used. For a PCCVS with two probes, the output behavior is defined as:

$$v_{\mathrm{out}} = p_0 + p_1 i_1 + p_2 i_2 + p_3 i_1^2 + p_4 i_1 i_2 + p_5 i_2^2, \qquad (4)$$

where p_m is the m-th polynomial coefficient and i_n is current measured by the n-th probe. Therefore, to have the PCCVS output $-\omega L_{\mathrm{f}} i_{\mathrm{q}}$, probe 1 measures ω, probe 2 measures i_{q} and all polynomial coefficients are 0 except for $p_4 = -L_{\mathrm{f}}$. The development for the $\omega L_{\mathrm{f}} i_{\mathrm{d}}$ value dependent voltage source in the Q-axis follows the same approach.

The dependent current sources in parallel with the filter capacitor are modeled using the voltage controlled current source (VCCS) in Virtuoso. While it may seem that these sources are dependent on a voltage and a current, the value of ω_{g} is fixed. Thus, the VCCSs use the voltages on the secondary-side of the transformers as inputs and have defined gain values of $\omega_{\mathrm{g}} C_{\mathrm{f}}$ to produce the dependent currents depicted in Fig. 1(b).

E. Electrical Network Transmission Lines

Transmission lines that interconnect the inverters in the electrical network are modeled as series RL circuits with dynamics represented in the global DQ reference frame. For simplicity of notation and without loss of generality, all inductances and resistances are assumed to be equal and given by L_{g} and R_{g}, respectively. The line impedance between buses on both the D-axis and Q-axis is represented as the series combination of an inductor L_{g}, a resistor R_{g}, and a dependent voltage source.

Following the methods above, these line impedances are realized in Virtuoso with ideal inductors, ideal resistors, and CCVSs. It is important to note that for a SPICE-based simulator, there cannot be two sources directly connected in series with each other. To overcome this obstacle, an arbitrarily small resistance (picked to be $1[\mathrm{n}\Omega]$ in our simulations), is placed between the two sources to isolate them.

III. Network Simulations

In this section, we present the distribution network modified from the IEEE 118-bus system. The network is constructed and simulated within PLECS, a power electronics simulation software, and Virtuoso. We then make comparisons between the two simulations to determine trade-offs.

A. 118 Bus Network Implementation

The network comprises 54 individual inverters and 91 loads (see Fig. 2). Inverters are realized in Virtuoso using the

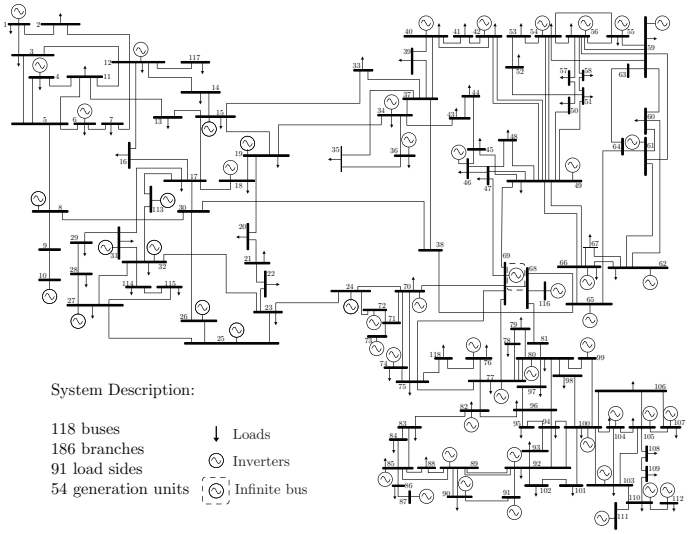


Fig. 2. One-line diagram of the modified IEEE 118-bus test system illustrating locations of inverters, loads, and the infinite bus.

equivalent-circuit inverter model presented in Section II. The loads are modeled as series RL circuits designed to consume the aggregate amount of power produced by the 54 inverters rated at 1000 [VA] each. A single bus within the network was chosen to represent the connection to the bulk power grid in the form of an infinite bus. In the global DQ frame, this is modeled with DC voltages $E_{\mathrm{D}} = 240/\sqrt{2}$ [V], $E_{\mathrm{Q}} = 0$.

B. Simulation Details

Transient simulations for period 0.2 [s] are performed in PLECS and Virtuoso. The initial conditions of each simulation are set to the steady-state conditions of the respective system from 0 to 0.05 [s]. The reference current $i_{\mathrm{d}}^{\star}$ for each individual inverter was randomly chosen to be one of three possible options: i) $i_{\mathrm{d}}^{\star}$ = 5 [A] for 0.05 [s] then steps to 15 [A]; ii) $i_{\mathrm{d}}^{\star}$ = 0 [A] for 0.10 [s] then steps to 10 [A]; iii) $i_{\mathrm{d}}^{\star}$ = 15 [A] for 0.15 [s] then steps to 5 [A]. The reference current $i_{\mathrm{q}}^{\star}$ is held to 0 [A]. To ensure fairness, the maximum time step and relative tolerance in both simulations are set to 10^{-4} and 10^{-3}, respectively. In PLECS, the solver used for the simulation is the variable-step RADAU stiff solver. The Virtuoso network model is simulated using Cadence Spectre, a SPICE-based simulator, with the second-order Gear's method solver.[1]

C. Comparison of Accuracy and Computation Speed

The per-unit mean squared difference between the voltage time series outputs in SPICE versus those in PLECS are calculated for the D-axis and Q-axis voltages at every node in the network across the simulation horizon and shown in Fig 3. The average mean squared difference is 4.73×10^{-6}, and it indicates that the PLECS solver and the SPICE solver

[1]Simulation parameters are as follows: Nominal frequency, $\omega_{\mathrm{nom}} = 2\pi 60$ [rad/s]; Filter inductance $L_{\mathrm{f}} = 1.5$ [mH]; Filter resistance $R_{\mathrm{f}} = 0.5$ [Ω]; Filter capacitance $C_{\mathrm{f}} = 10$ [μF]; Line inductance $L_{\mathrm{g}} = 0.1$ [mH]; Line resistance $R_{\mathrm{g}} = 0.1$ [Ω]; Proportional gain of CC, $k_{\mathrm{CC}}^{\mathrm{p}} = 2.83$ [V/A]; Integral gain of CC, $k_{\mathrm{CC}}^{\mathrm{i}} = 942$ [V/(As)]; Proportional gain of PLL, $k_{\mathrm{PLL}}^{\mathrm{p}} = 5$ [rad/(Vs)]; Integral gain of PLL, $k_{\mathrm{PLL}}^{\mathrm{i}} = 10$ [rad/(Vs)^2].

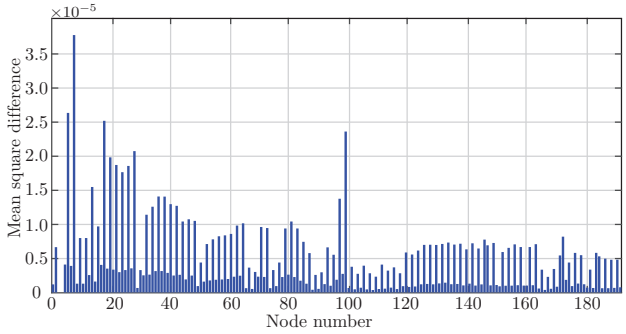


Fig. 3. Per-unit mean squared difference for nodal D- and Q-axis component voltages in the 118-bus network across the 0.2 [s] simulation horizon.

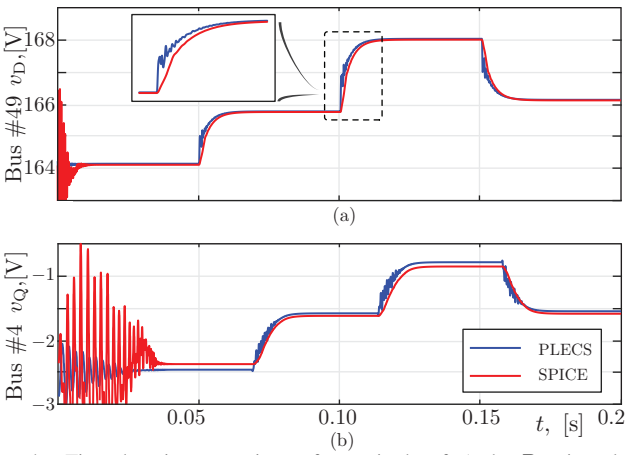


Fig. 4. Time-domain comparison of magnitude of a) the D-axis voltage component at Bus 49, and b) the Q-axis voltage component at Bus 4.

produce approximately the same results at every bus in the network. Further investigation reveals that SPICE waveforms sacrifice resolution for speed, as they appear to be smoothed versions of PLECS waveforms during transients triggered by changes in reference current values. The steady state values in each case are approximately the same. (See Fig. 4 for representative time-domain comparisons.) While the SPICE simulation produces a lower resolution result, the increase in simulation speed is marked. Ignoring the initial transient, the average total simulation time of the 118-bus system in SPICE over 3 trials is 10.15 [s] as measured by the Spectre console. The average simulation time measured by the PLECS console over 3 simulations is 3641.04 [s].

IV. Conclusions and Future Work

In this paper, we demonstrated how the equivalent-circuit representation of a three-phase grid-following inverter and a networked collection of such inverters can be implemented within a SPICE environment. Simulation results demonstrated comparable accuracy with computational savings. Future work involves developing scripts that automate the process of laying out large inverter networks within Virtuoso using Cadence SKILL and investigating other complex power-electronics inverter topologies, control methods, and network configurations. Investigating other solvers to gauge computational benefits is also critical to establish a comprehensive comparison across platforms and simulation approaches.

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