Decentralized PWM Interleaving for Ripple Minimization in both Symmetric and Asymmetric Parallel-connected DC-DC Converters

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***Abstract*—A decentralized control technique for minimizing the input and output current ripple in parallel connected dc-dc converters under both uniform and non-uniform operating conditions is presented in this paper. We solve two key problems related to obtaining minimum ripple operation of these converters. First, we eliminate the need for a centralized controller that manages system-wide pulse width modulation. This yields a decentralized structure where converters autonomously converge to the operating point with minimized ripple using only local voltage feedback. Second, we obtain a controller that can function in the presence of parametric mismatches as well as nonuniformities in converter duty ratios that naturally arise with heterogeneous input sources. More precisely, the proposed controller minimizes the fundamental switching harmonic under both uniform and asymmetric operating conditions. For the case studies we consider, a more than $4\times$ reduction in net current ripple is observed compared to conventional methods. Moreover, the undesired fundamental harmonic is reduced by more than 30 dB. Relevant analysis, simulation results and experimental results with 5 parallel-connected dc-dc converters validate the proposed method.**

I. Introduction

Systems of parallel-connected dc-dc converters are ubiquitous across applications. Architectures with parallel-connections on both the inputs and outputs (see Fig. 1(a)) are generally referred to as *multiphase* converter systems are often seen in computing applications. Setups with independent inputs and parallelized output interconnections (see Fig. 1(b)) appear in many applications from dc microgrids to mobile devices. This configuration is often called a *point-of-load* system. Although current ripple is an unavoidable in any system with power electronics, we can use the notion of switch interleaving to obtain ripple cancellation once currents sum together. However, the fact that interleaving requires control of the relative switch timing among converters creates challenges. For instance, as the number of converters goes up we eventually run into channel count and computational resource limitations on any given digital controller. Hence, centralized control architectures cannot be extended to systems with arbitrarily large converter counts. Furthermore, any source of asymmetry among converters obscures what phase shifts are needed between converter switch edges for ideal ripple cancellation. In this paper, we propose, analyze, and experimentally demonstrate a decentralized control strategy where dc-dc converters with independent control loops can be interconnected in various configurations while giving robust ripple cancellation.

Multiphase systems as shown in Fig. 1(a) offer several key performance advantages that make them the default choice for high current applications. Advantages include relaxed input and output capacitance requirements, dispersed heat dissipation, improved efficiency at high currents, and enhanced dynamic performance. These benefits are compounded as the number of paralleled units increases. In general, when N converters operate under uniform conditions at their inputs and outputs, then evenly dispersed phase shifts of $360^\circ/N$ between periodic switch edges yields minimum net ripple. This condition, which is known as *symmetric interleaving*, yields minimized net ripple only under this ideal setting and is mainly applicable to multiphase dc-dc systems with modest numbers of converters. Generally speaking, any source of non-uniformity degrades ripple cancellation if symmetric interleaving is maintained. For instance, unavoidable parametric mismatches among filter inductances reduces ripple cancellation [1]. Going one step further and looking at systems with non-uniformly rated modules and decoupled inputs, as shown in Fig. 1(b), the extent of non-uniformity only goes up. In such scenarios, mismatches among the input-side voltages naturally lead to nonuniform duty ratios among the converters. In this paper, we seek a control strategy that not only gives us a high degree of ripple cancellation under asymmetries, but also lends itself to a decentralized control implementation such that arbitrarily-sized systems can be assembled for various applications.

Considering the discussion above, it should no wonder that ripple cancellation in heterogeneous systems has been a focus of recent investigations. Previous work on this front has mostly been centered on centralized controllers [2]–[8] that compute optimal phase shifts. Note that these methods impede scalability due to the centralized implementation. Moreover, methods proposed in [4]–[9] are based on controllers and algorithms which have considerable computational burden and often rely

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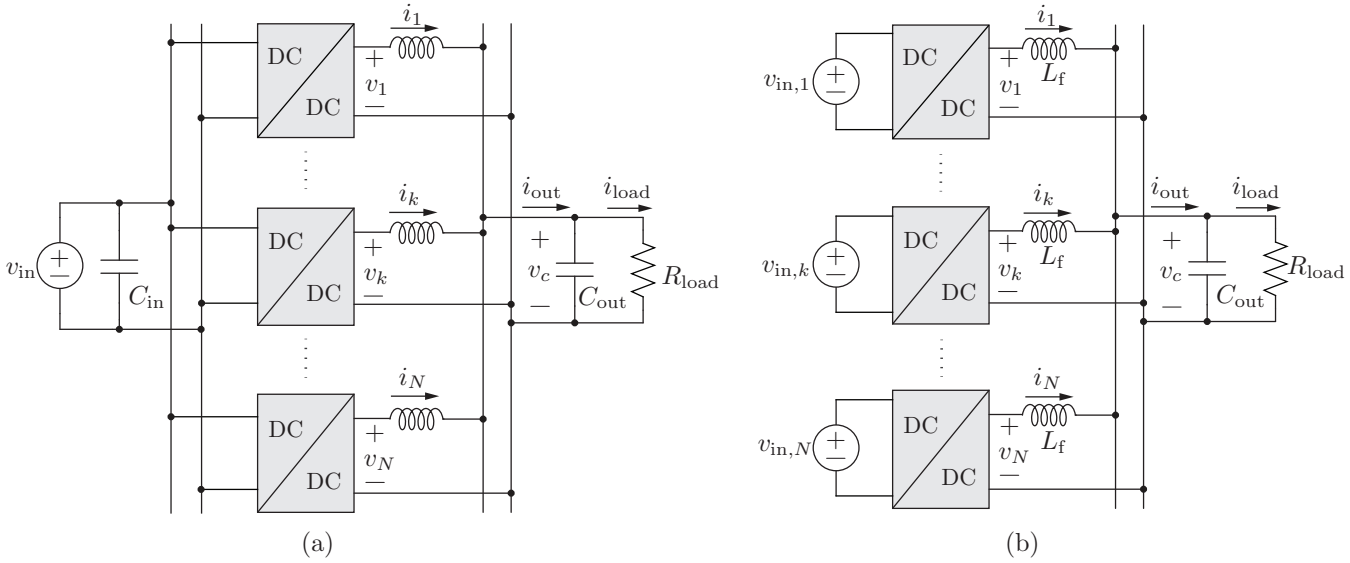


Fig. 1. System architecture of parallel-connected DC-DC converters: (a) Parallel-input parallel-output multi-phase system. (b) Parallel-output converter system with non-uniform decoupled input sources.

on look-up tables that introduce further complexities. For instance, the optimization result and system under consideration in [6]–[8] is limited to only 3 modules. Decentralized control for ripple minimization in multi-converter systems had been investigated in [9]–[13]. Note that the work in [9] gives a decentralized interleaving controller for parallel connected buck converters, but is only shown to handle identical converters and relies on a high sample rate which impedes implementation. Recently, the work in [10] shows an optimization technique for decentralized asymmetric dc-ac inverters. This paper addresses several of the key drawbacks of prior works and takes the deceptively simple form of a proportional controller. We call this the *Asymmetric Phase Shift Controller* (APSC). The key innovation needed to uncover this elegant implementation lies in the timing of the sampling instant of the output capacitor voltage. In summary, we show that a measurement taken at a precisely chosen time-instant captures all information needed for decentralized feedback control and convergence to the phase shifts which minimize net switching ripple. This property holds irrespective of any non-uniformity in the system.

Hereafter, the paper is organized as follows: Section II outlines notation and establishes foundational analysis for the quantification of ripple harmonics. Next, the controller is formulated in Section III and its closed-loop dynamics are characterized. Simulation and experimental results follow in Section IV and concluding statements appear in Section V.

II. System Modelling and Fourier Analysis of Output Capacitor Voltage

As shown in Fig. 1(b), we consider N asymmetric multi-phase dc-dc converters connected in parallel at their output and collectively delivering power to a common load R_{load} across a capacitor C_{out}. The set $\mathcal{N}$ is defined as $\mathcal{N} := \{1, 2, \cdots, N\}$ and $v_{\text{in},k}$ is the input supply for the k^{th} converter. A triangular waveform for the k^{th} converter inductor current $i_k(t)$ is shown in Fig. 2. The ac ripple component of $i_k(t)$, denoted as $\widetilde{i}_k(t)$, can be expressed as the Fourier series

$$\widetilde{i}_k(t) = \sum_{m=1}^{\infty} A_{k,m} \cos((m(\omega_{\text{sw}} t - \phi_k) - \psi_{k,m}), \tag{1}$$

$$= \sum_{m=1}^{\infty} A_{k,m} e^{-j\theta_{k,m}}, \tag{2}$$

where, $A_{k,m}$ and $\psi_{k,m}$ denote the magnitude and phase of the m^{th} harmonic component. ϕ_k is the phase shift of the k^{th} converter PWM pulse with respect to a frame synchronously rotating at angular velocity $\omega_{\text{sw,nom}}$. Therefore, the total ripple current to be absorbed by the output capacitor, $\widetilde{i}_{\text{out}}$, is

$$\widetilde{i}_{\text{out}}(t) = \sum_{k=1}^{N} \widetilde{i}_k(t), \tag{3}$$

$$= \sum_{k=1}^{N} \sum_{m=1}^{\infty} A_{k,m} \cos\left(m(\omega_{\text{sw}} t - \phi_k) - \psi_{k,m}\right). \tag{4}$$

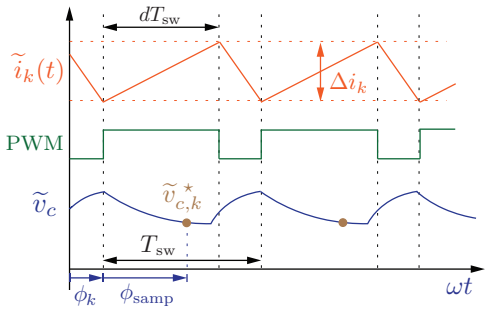


Fig. 2. Switching-level diagram of inductor current of the k^{th} phase.

In subsequent work, we consider the fundamental switching frequency harmonic in this current since that is the most significant component in the ripple absorbed by the capacitor. Hence, this component largely determines the capacitor size. From here onward, we drop the subscript m representing the harmonic order. From (4), the fundamental switching component is

$$\widetilde{i}_{\text{out},1}(t) = \sum_{k=1}^{N} A_k \cos\left((\omega_{\text{sw}} t - \phi_k) - \psi_k\right) = \sum_{k=1}^{N} A_k e^{-j\theta_k}. \tag{5}$$

The above can also be expressed in polar form where, $\theta_k = \phi_k + \psi_k$. From (5), the fundamental harmonic in the capacitor voltage ripple is

$$\widetilde{v}_{c,1} = \frac{1}{C_{\text{out}}} \int \widetilde{i}_{\text{out},1}\, dt, \tag{6}$$

$$= \sum_{k=1}^{N} B_k \sin\left((\omega_{\text{sw}} t - \phi_k) - \psi_k\right), \tag{7}$$

$$= \sum_{k=1}^{N} B_k e^{-j\theta_k} = B_r e^{-j\theta_r}, \tag{8}$$

where $B_k = A_k/(\omega_{\text{sw}} C_{\text{out}})$ and B_r is the net 1st harmonic ripple amplitude produced by the N converters with phase θ_r. For the purpose of digital implementation in each switch cycle, the k^{th} converter samples the output terminal voltage at an angle ϕ_{samp} of its switching period. This translates to sampling the output capacitor voltage waveform at $\omega_{\text{sw}} t = \phi_{\text{samp}} + \phi_k$ (see Fig. 2). Therefore, from (8), the sampled fundamental ripple voltage observed by the k^{th} converter in the n^{th} switching cycle, denoted as $\widetilde{v}^{\star}_{c,k}$, is

$$\widetilde{v}^{\star}_{c,k}(nT_{\text{sw}}) \approx \sum_{l=1}^{N} B_l \sin\left((\phi_{\text{samp}} + \phi_k) - \phi_l - \psi_l\right), \tag{9}$$

$$\approx \sum_{l=1}^{N} B_l \sin\left(\phi_{kl} + \phi^{\star}\right), \tag{10}$$

where $\phi_{kl} = \phi_k - \phi_l$ and $\phi^{\star} = \phi_{\text{samp}} - \psi_l$.

III. Proposed Decentralized Asymmetric Phase-Shift Control (APSC) Method

As shown in (8), the fundamental harmonic component contributed by each converter is represented as a phasor with amplitude B_k and phase θ_k relative to the synchronously rotating frame with angle $\omega_{\text{sw}} t$. This is pictorially depicted in Fig. 3. The sum of all such phasors is the net resultant phasor with amplitude B_r and phase θ_r. Note that the first harmonic is completely eliminated iff, $B_r = 0$. However, if there are system asymmetries then each converter generates unequal ripple amplitudes B_k, $(k \in \mathcal{N})$. In such scenarios there might not be any set of angles, θ_k, $(k \in \mathcal{N})$, that give complete cancellation of the first harmonic. Therefore, our objective is to minimize B_r for any condition. This can be done by controlling the harmonic phases θ_k, $(k \in \mathcal{N})$, by

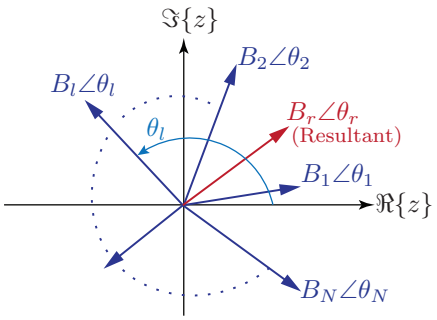


Fig. 3. Harmonic phasor diagram of capacitor voltage.

modulating the PWM phase-shift angles ϕ_k, $(k \in \mathcal{N})$. For this purpose, we then choose our objective function as B_r^2 which is a quadratic potential function and is convex over ϕ_k, $(k \in \mathcal{N})$. In order to account for the effect of the sampling instant on the convergence of the controller, we express the potential function as

$$U(\phi) = B_r^2 \cos\phi^{\star}. \tag{11}$$

Now we seek a controller that drives the PWM carrier phases, ϕ_k, $(k \in \mathcal{N})$, towards the minimum fundamental harmonic state from any initial condition. We do this by constructing a potential-gradient-based control law that asymptotically drives $U(\phi)$ towards its global minimum [14], [15]. In particular, the phase of the k^{th} carrier is dynamically changed according to the negative of the potential gradient as

$$\dot{\phi}_k = -K_P \frac{\partial U(\phi)}{\partial \phi_k}, \quad \forall\, k \in \mathcal{N}, \tag{12}$$

where K_P is the controller gain.

A. Controller Implementation

Now we derive a practically implementable form of the gradient-based control law. The partial derivative in (12) captures the gradient of $U(\phi)$ in the direction of θ_k changes and can be evaluated by taking the inner product of the resultant vector $\vec{B}_r$ and the unit vector along the direction of θ_k denoted as $\hat{\theta}_k$. This gives

$$\frac{\partial U(\phi)}{\partial \phi_k} = \frac{\partial B_r^2 \cos\phi^{\star}}{\partial \theta_k} = \frac{\partial \langle \vec{B}_r\,,\, \vec{B}_r e^{-j\phi^{\star}} \rangle}{\partial \theta_k} \tag{13}$$

$$= 2\langle \vec{B}_r\,,\, \hat{\theta}_k e^{-j\phi^{\star}} \rangle \tag{14}$$

$$= 2\left\langle \sum_{l=1}^{N} B_l e^{-j\theta_l}\,,\, -j e^{-j(\theta_k + \phi^{\star})} \right\rangle \tag{15}$$

$$= -2 \sum_{l=1}^{N} B_l \sin\left(\phi_{kl} + \phi^{\star}\right) \tag{16}$$

where, $\langle \cdot, \cdot \rangle$ represents the inner product of two quantities. It follows that

$$\dot{\phi}_k = 2K_P \times (\text{Sampled value of fundamental voltage ripple, } \widetilde{v}^{\star}_{c,k} \text{ as shown in (10)}). \tag{17}$$

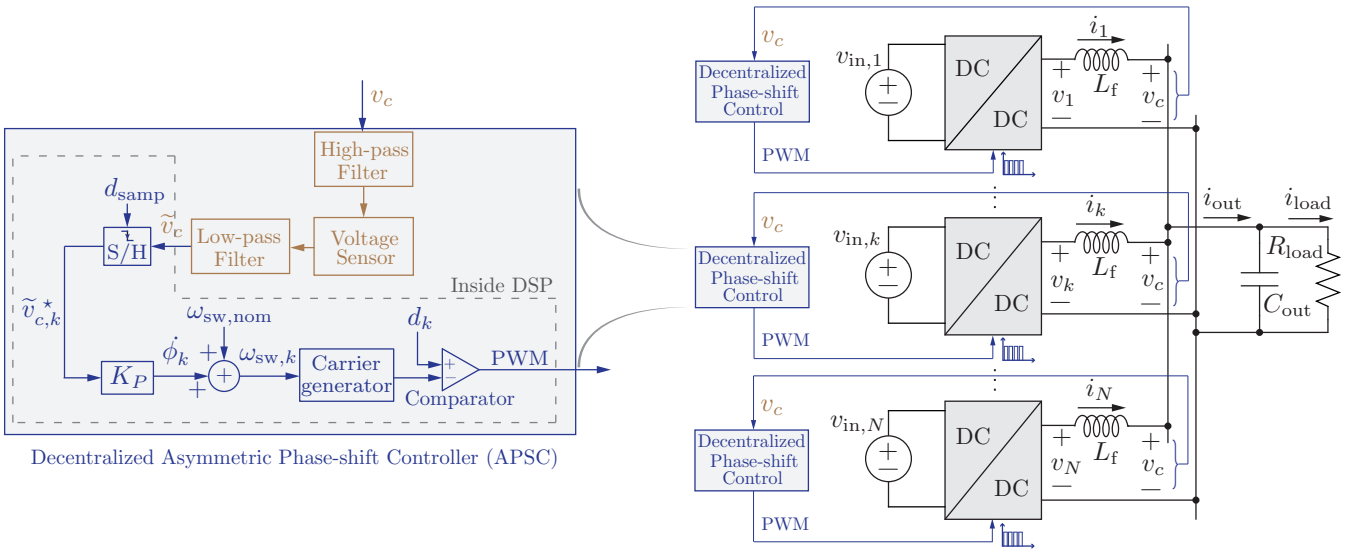


Fig. 4. Detailed illustration of decentralized Asymmetric Phase-shift Control (APSC) for N parallel connected DC-DC converters.

Figure 4 shows the hardware implementation of the control law in (17). The capacitor voltage is available for measurement at every set of converter terminals. An analog RC filter is used to remove the dc component from this voltage, which is then sensed by a voltage sensor and passed through a low-pass filter to attenuate the frequency components above the fundamental switching frequency. Then the output of the low-pass filter is sampled at a particular sampling instant d_{samp}. Next, the sampled voltage is multiplied by K_P and added to the nominal switching frequency of the system $\omega_{\text{sw,nom}}$. This perturbation in the switching frequency is used to adjust the PWM phase of the converter.

B. Selection of Measurement Sampling Point

At first glance, the control structure in Fig. 4 may seem obvious due to its simplicity. However, the key ingredient that has obscured its discovery by others and lies at the crux of its feasibility is the selection of the time instant at which the measurement is sampled. Here we show that if the sample is taken during a particular window of time, then the measurement contains all necessary information for feedback control and system-wide convergence to the potential function minimum. Next, we show how the proper sampling window is computed.

In any condition, the global minimum of B_r is ≥ 0. For the above controller to converge, then $U(\phi) \geq 0, \forall\, \phi = [\phi_1, \cdots, \phi_N]$ must be satisfied. Hence, we need $\cos\phi^{\star} > 0$ which further implies $-\pi/2 < \phi^{\star} < \pi/2$. Ultimately this gives the following inequality:

$$-\frac{\pi}{2} < \phi_{\text{samp}} - \psi_k < \frac{\pi}{2}, \quad \forall\, k \in \mathcal{N}. \tag{18}$$

Evaluating the Fourier series of i_k, we obtain $\psi_k = \pi d_k$. Using $\phi_{\text{samp}} = 2\pi d_{\text{samp}}$ in (18) gives

$$\frac{d_k}{2} - \frac{1}{4} < d_{\text{samp}} < \frac{d_k}{2} + \frac{1}{4} \tag{19}$$

In theory, the available range for selecting d_{samp} that satisfies this constraint must span across 0.5 in width. However, since the low-pass filter cannot completely eliminate the higher order harmonics, these harmonics inevitably sneak in and limit the sampling range. Furthermore, the low pass filter bandwidth also plays a significant role in determining the d_{samp} interval. The phase lag introduced by the low-pass filter at the fundamental harmonic component shifts the required sampling interval and, hence, needs to be characterized. It should be noted that the bandwidth of the voltage sensor does not play a significant role in the controller performance and any off-the-shelf voltage sensor can be used for this purpose.

IV. Simulation & Experimental Results

A. Simulation Results

In order to validate the performance of the proposed method, 3 case studies with $N = 5$ parallel buck converters have been performed. The system parameters are listed in Table I.

Case 1: Figure 5 shows controller performance for a uniform system with equal input voltages and filter inductance. Figure 5(a)-(b) illustrates convergence of the controller to the symmetric interleaved state for $V_{\text{out}} = 30V$ and Fig. 5(c)-(d) shows similar results for $V_{\text{out}} = 70V$.

TABLE I
System and Controller Parameters in Simulations

Symbol	Description	Value	Units
v_{in}	Nominal input voltage	100	V
f_{sw}	Nominal switching frequency	20	kHz
C_{out}	Output Capacitance	10	μF
R_{load}	Load resistance	2.5	Ω
L_{f}	Filter inductance	100	μH
K_P	APSC Controller gain	50	Hz/V

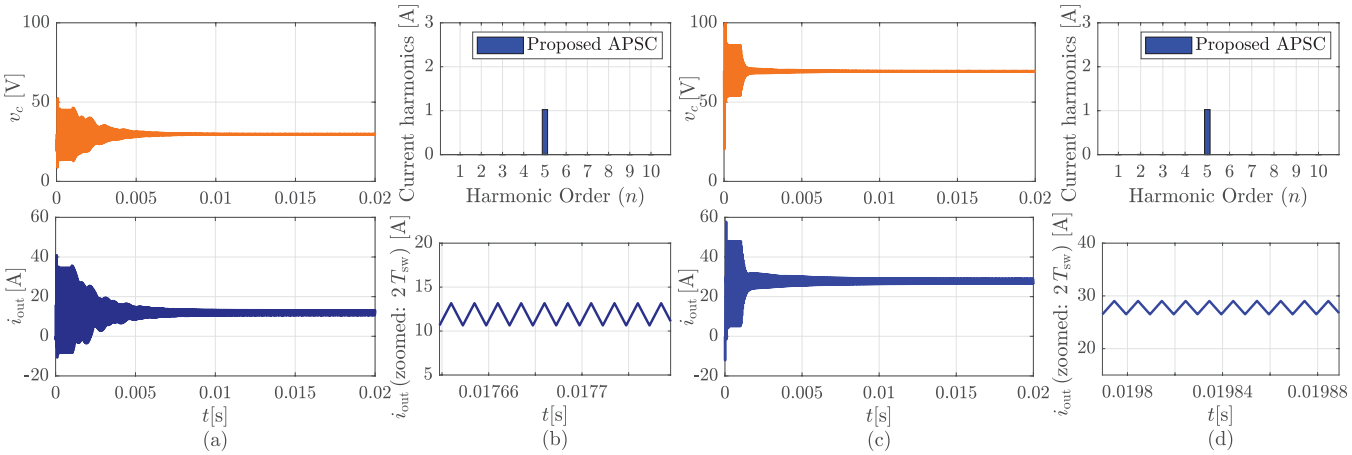


Fig. 5. Simulation results for Case 1: Uniform system. Output capacitor voltage (top) and output current (bottom), Harmonic content in capacitor current (top) and enlarged view of current ripple (bottom). For (a)-(b) $V_{\text{load}} = 30\,V$ and (c)-(d) $V_{\text{load}} = 70\,V$.

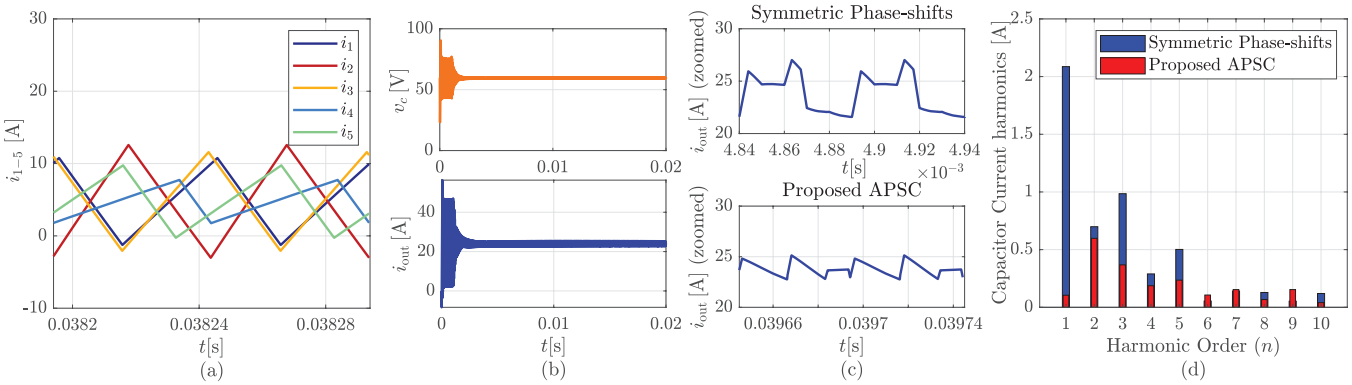


Fig. 6. Simulation results for Case 2: Non-uniform input voltages. $v_{\text{in},1} = 100\,V$, $v_{\text{in},2} = 125\,V$, $v_{\text{in},3} = 110\,V$, $v_{\text{in},4} = 75\,V$ and $v_{\text{in},5} = 85\,V$. (a) Module inductor currents, (b) Capacitor voltage and output current. Comparison of conventional symmetric phase-shift and proposed APSC for: (c) Enlarged view of current ripple, (d) Harmonic content in capacitor current.

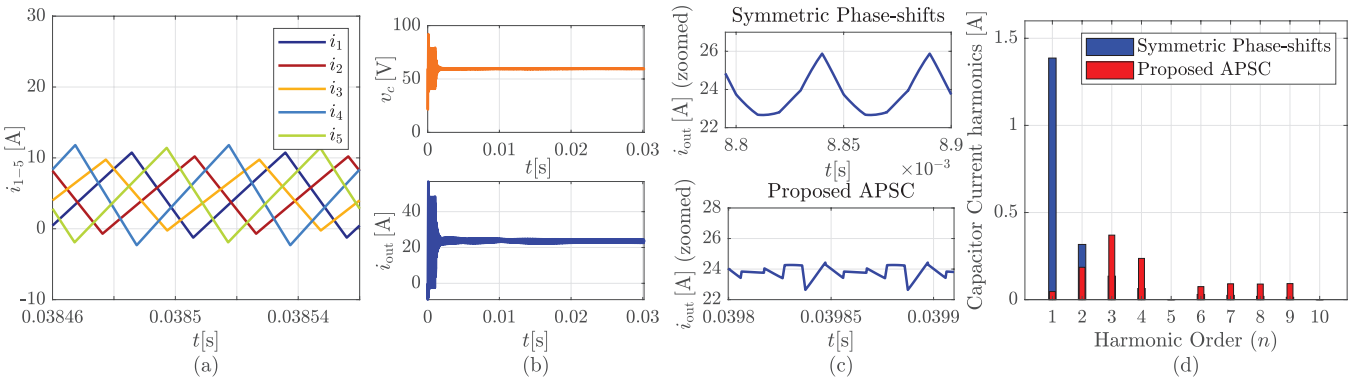


Fig. 7. Simulation results for Case 3: Non-uniform filter inductances. $L_{\text{f},1} = 100\,\mu\text{H}$, $L_{\text{f},2} = 110\,\mu\text{H}$, $L_{\text{f},3} = 120\,\mu\text{H}$, $L_{\text{f},4} = 85\,\mu\text{H}$ and $L_{\text{f},5} = 90\,\mu\text{H}$. Plots in (a)-(d) has similar description as Fig. 6.

Case 2: Now we demonstrate the effectiveness of the proposed controller over symmetric phase-shift interleaving when the converters operate with different input voltages ($\pm\,25\%$ variation). Figure 6(a) shows the unequal currents in the 5 units and Fig. 6(b) shows the convergence of the output capacitor voltage and currents to the minimum ripple state. Figure 6(c) compares the output current ripple with conventional symmetric phase-shifts and proposed control. Next, Fig. 6(d) shows the harmonic content in the capacitor current in these two cases. As can be seen proposed controller gives almost complete elimination of the fundamental harmonic component and results in over $3\times$ reduction of the overall

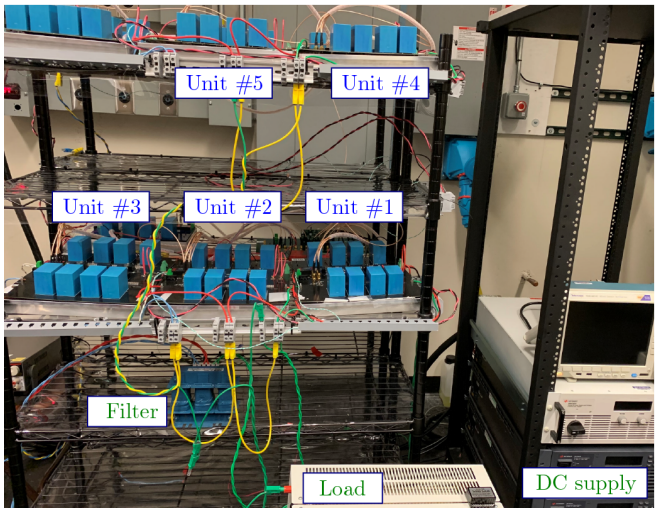


Fig. 8. Experimental setup of 5 parallel connected dc-dc converters.

harmonic content in the capacitor current.

Case 3: This case study shows the effectiveness of APSC method with ± 20 % tolerance in the filter inductances of the modules which is very common in practical scenarios. Fig. 7(a)-(d) shows similar results as Fig. 6 and in this case, the APSC method result in 30 dB reduction in the fundamental harmonic component and 2.4× reduction in the overall harmonic content in the capacitor current.

B. Experimental Results

A hardware setup consisting five parallel-connected dc-dc converters is shown in Fig. 8. Each converter has a dual active bridge (DAB) input stage followed by an output buck converter. The outputs of the buck stages are connected in parallel across a resistive load. The input sides of the DABs are all in parallel across a common dc supply. Each DAB output is controlled to provide a selectable voltage to its respective buck input. The setup is shown in Fig. 8. Each converter is controlled by a dedicated TMS320F28379D digital signal processor and has independent voltage sensing circuitry. The hardware and control parameters are in Table-II.

TABLE II
SYSTEM AND CONTROLLER PARAMETERS IN EXPERIMENTS

Symbol	Description	Value	Units
V_{in}	Dc supply input voltage	100	V
v_{in}	Nominal buck input voltage	50	V
f_{sw}	Switching frequency	10	kHz
C_{out}	Output capacitance	25	μF
R_{load}	Load resistance	5	Ω
L_{f}	Phase inductance	230	μH
K_P	Controller gain	50	Hz/V
–	Low-pass filter bandwidth	20	kHz

Figure 9 shows measurements when the system operates with uniform input voltages and hardware parameters while regulating 12 V across the load. In this case, the controller converges to the symmetric interleaved state. The transient

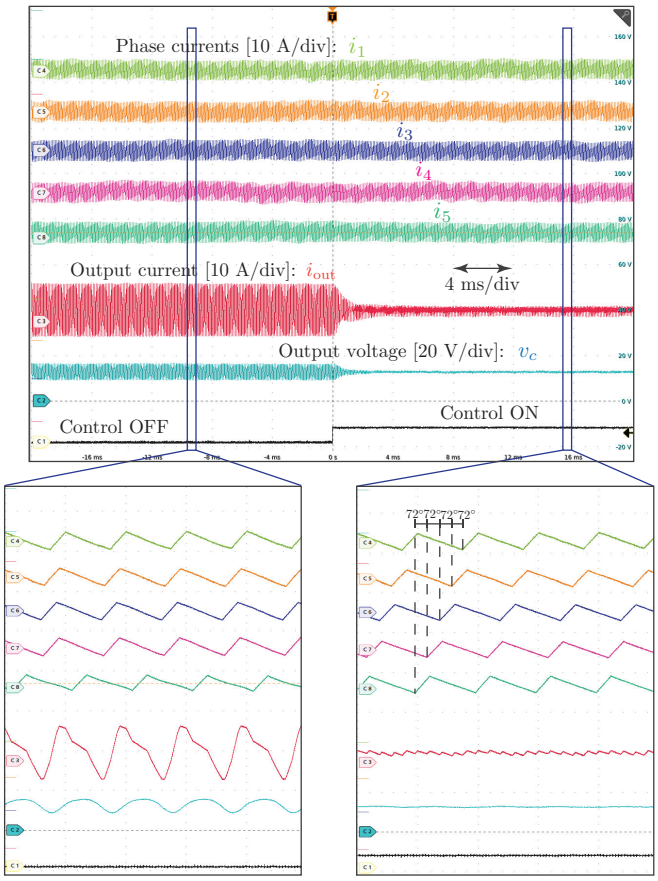


Fig. 9. Measured waveforms of phase currents, load current, and load voltage during operation with uniform power stage voltage inputs and average current delivery.

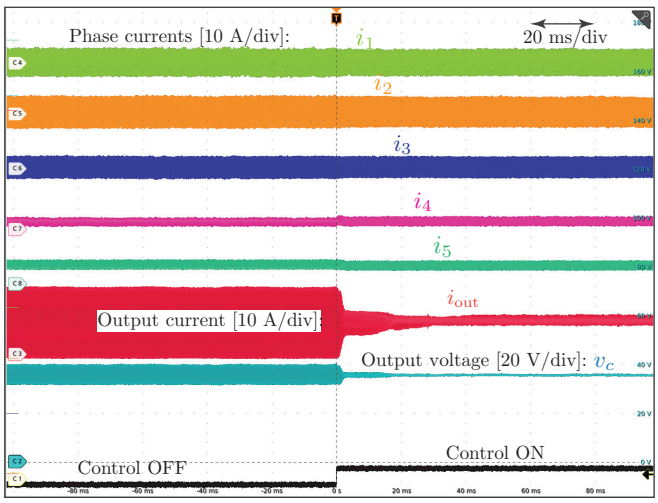
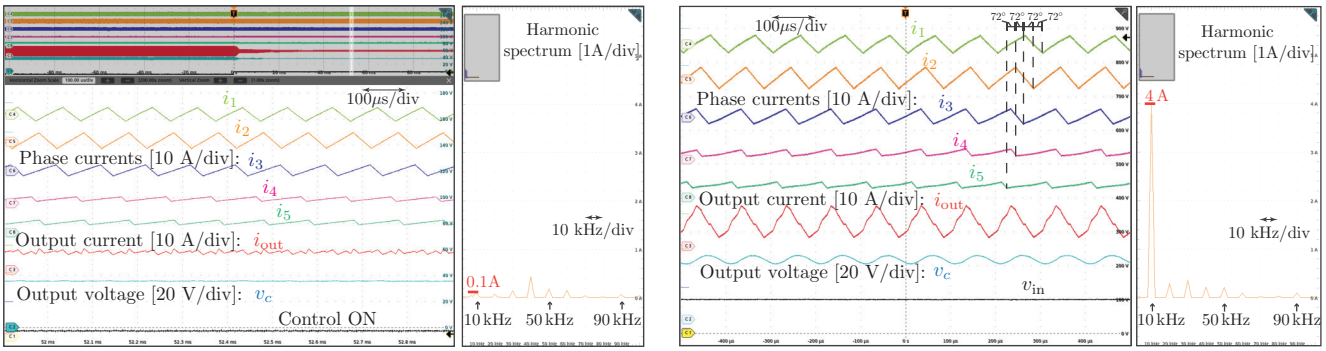


Fig. 10. Experimental validation with non-uniform input voltages. Convergence to the minimized ripple state from arbitrary initial conditions is obtained in 40 ms.



(a) Proposed APSC Method

(b) Symmetric Interleaving

Fig. 11. Experimental validation of the proposed APSC in case of non-uniform input voltages. A 4.5× net reduction in the output current ripple is obtained in (a) compared to the symmetric interleaving in (b).

response of the controller is depicted before and after the controller is turned on. Convergence to the interleaved state occurs within around 4 ms. Evidently, the peak-to-peak ripple in i_{out} reduces from 12 A to 2 A for a 6× reduction. The worst case current ripple appears when the PWM carriers become phase-synchronized due to drifts among DSP clocks. Hence, ripple reduction for such a condition would be even higher.

Transients under non-uniform input voltages where $v_{\text{in},1} = 58\,V$, $v_{\text{in},2} = 60\,V$, $v_{\text{in},3} = 50\,V$, $v_{\text{in},4} = 40\,V$ and the load voltage is $V_{\text{load}} = 36\,V$ are in Fig. 10. Here, the closed-loop system converges to the minimum ripple state in 40 ms. The output voltage was sampled at $d_{\text{samp}} = 0.1$. Figures 11(a) and (b), respectively, show the steady-state phase currents, i_1 through i_5, output current, i_{out}, capacitor voltage, v_c, as well as the harmonic spectrum of i_{out} under both the proposed control and conventional symmetric interleaving. The total harmonic content in i_{out} is reduced by 4.5× as it fell from 5.4 A to 1.2 A. Note that the 1st harmonic component is attenuated from 4 A to 0.1 A for a −32 dB reduction compared to symmetric interleaving.

Performance with mismatched filter inductances is illustrated in Fig. 13. In particular, the buck output inductances were selected as $L_{\text{f},1} = 460\,\mu\text{H}$, $L_{\text{f},2} = 230\,\mu\text{H}$, $L_{\text{f},3} = 115\,\mu\text{H}$, $L_{\text{f},4} = 345\,\mu\text{H}$, and $L_{\text{f},5} = 230\,\mu\text{H}$. The output

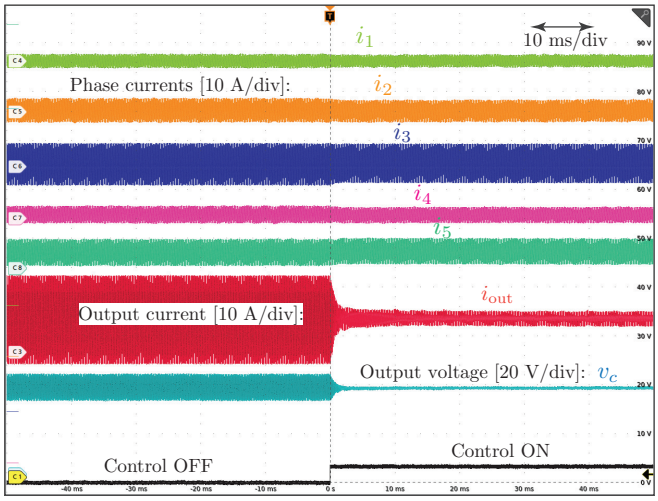
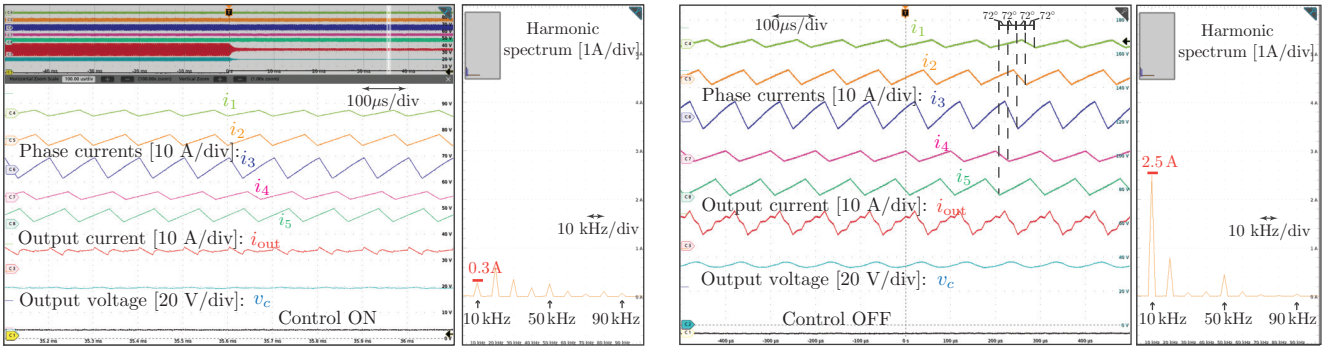


Fig. 13. Measurements with asymmetric filter inductances. Convergence to the minimized ripple state occurs within 10 ms.



(a) Proposed APSC Method

(b) Symmetric Interleaving

Fig. 12. Experimental validation of proposed APSC in case of asymmetric filter inductances. A 2× net reduction in the output current ripple is obtained in (a) compared to the symmetric interleaving in (b). The fundamental switching harmonic is attenuated by −18 dB.

voltage is regulated at 36 V. Output currents converge to the minimized ripple state within approximately 10 ms and the $d_{\text{samp}} = 0.1$. Figures 12(a) and (b), respectively, show steady-state waveforms and the harmonic spectrum of i_{out} for both the proposed control and symmetric interleaving. Superior performance of the proposed method is evident despite the challenges brought on by asymmetries. Note that harmonics in i_{out} went from 4.2 A to 2.1 A for a $2\times$ reduction. Compared to symmetric interleaving, the proposed controller reduced the 1^{st} harmonic amplitude fell from 2.5 A to 0.3 A for an -18 dB reduction.

V. Conclusion

In this paper, we proposed and validated a decentralized controller that modulates PWM carrier phase shifts for current ripple minimization in parallel-connected dc-dc converters. The proposed method works for both symmetric and asymmetric parallel-connected setups. Reduced current ripple absorbed by the output capacitance also reduces the current rating and size of the filter capacitor such that power density is enhanced, distortion is mitigated, and efficiency increases. The proposed controller samples the locally-sensed terminal voltage in each switch cycle and functions by perturbing the switching frequency of the converter around it's nominal value in proportion to the sensed ripple content. Compared to prior methods, our approach is fully decentralized and is much simpler to implement as it does not entail complex optimization algorithms, look-up tables, sophisticated sensing, and measurement oversampling. Finally, performance gains offered by the proposed method were experimentally demonstrated on a parallel-connected setup of five dc-dc converters.

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