A Single-Stage Three-Phase AC Module for High-Voltage Photovoltaics

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***Abstract*—A single-stage three-phase voltage source inverter for high-voltage PV modules is presented. The benefits of the proposed design are simplicity, low cost, high efficiency, and high reliability. The inverter is intended for module integration and is designed for a relatively low power rating of approximately 250 W. Analytical models and dynamic simulation are used to calculate expected efficiency. The mean time to failure is estimated using established methods. Component costs are approximated with a linear regression which relates device ratings with price data. It is shown that in comparison to conventional single-phase module-integrated converters, the power component cost reduction is approximately 60%, peak efficiency is increased above 98%, and longer life is anticipated. Experimental results are shown.**

I. Introduction

Recent advances in photovoltaic (PV) cell technology include the development of microsystems-enabled PV (MEPV) cells [1]–[3] and micro-transfer printed PV cells [4] which can be used to create high-voltage PV modules. These types of PV cells are very thin and have small widths of 100 μm up to several mm. A module requiring very little semiconductor material can be produced when the cells are outfitted with an array of small optical concentrators. Due to minimal semiconductor requirements, module costs can be reduced substantially while yielding competitive efficiencies. Because each MEPV cell and its concentrating optics covers a small surface area, a complete module would consist of several thousand individual cells. An MEPV module with relatively high output voltage and low current can be constructed by connecting the cells in suitable series and parallel combinations [5]. Low output current is advantageous because conduction losses, which are proportional to the current squared, are reduced substantially and the high output voltage simplifies power electronic conversion by eliminating the need for a voltage boosting dc-dc converter.

A *microinverter* generally refers to an inverter designed to interface an individual PV module to the ac grid. The combination of a PV module and microinverter is called an *ac module*. Current research in ac modules has focused predominantly on single-phase power for residential applications. Because PV modules produce constant dc power in steady state and single-phase grid power is oscillating at twice the grid frequency, energy conservation requires the energy difference to be stored and released in decoupling capacitors [6]. Recent designs often use film decoupling capacitors instead of electrolytic capacitors which are prone to drying. However, the low energy-storage density of film capacitors results in a bulky and expensive decoupling stage. Furthermore, the filter and power electronic conversion stages add costs and limit efficiency.

Three-phase ac module design for commercial, industrial, and utility installations is relatively unexplored. Because the input and output power are both constant in a three-phase system, low-frequency decoupling capacitors are unnecessary. Costs can be reduced further by using a high-voltage MEPV module at the inverter input so that a voltage boosting stage is unnecessary. In [7]–[9], a low-power three-phase current source inverter (CSI) for high-voltage thin-film module integration demonstrated high efficiency and low cost. In [10], a three-phase ac module was developed but showed low efficiency. In this paper, a non-isolated three-phase ac module based on a voltage source inverter (VSI) topology is presented, analyzed, and demonstrated experimentally. The benefits of the proposed design are simplicity, low cost, high efficiency, and high reliability.

II. Three-Phase MEPV Inverter Description

The proposed inverter circuit is shown in Fig. 1. As bulk decoupling capacitance is not needed, the dc-link capacitor, C_{in}, is used solely to buffer the PV module from switching transients and maintain a small module voltage ripple. The capacitance requirement of 200 nF was determined using a dynamic model so that module ripple losses were less than 0.25% at rated power. For the VSI to be operational, the dc-link voltage, v_{pv}, must always exceed the peak ac voltage such that

$$v_{\text{pv}} > 2\sqrt{2}V_{\text{LN}} = 2\sqrt{\frac{2}{3}}V_{\text{LL}} \tag{1}$$

Table I summarizes the module voltage constraints with commonly available three-phase voltages in the US. The values

Table I
PV module voltage lower limits

V_{LL}	v_{pv} minimum
208 V	340 V
480 V	785 V

in Table I show that a 480 V grid voltage will require a PV module voltage of at least 785 V. A 208 V system could be accommodated with a more modest module voltage of 400 V.

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It is shown in [7] that a 400 V PV module could be interfaced with higher grid voltages, such as 480 V, if a CSI is used. The CSI inverter has a voltage boosting characteristic and the VSI acts as a voltage step-down converter. From here forward, it will be assumed that a 208 V system is used in conjunction with the three-phase VSI.

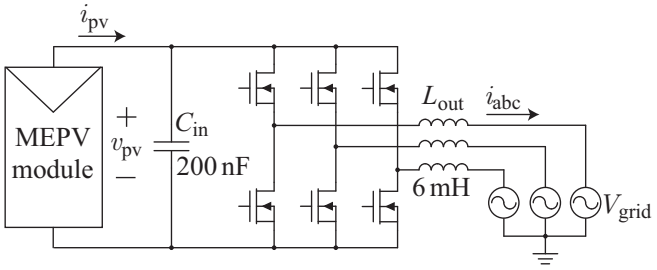

Figure 1. Proposed three-phase PV inverter

III. Control

The inverter controller is shown in Fig. 2. The module current and voltage are utilized by the maximum power point tracker (MPPT) which in turn generates a PV voltage command, v_{pv}^*. A PI controller ensures $v_{pv} \rightarrow v_{pv}^*$ by altering the magnitude of the phase current command, i_{pk}^*. The angle, θ, of the phase A voltage with respect to neutral, v_{an}, is determined by a phase-locked loop. The phase current commands i_a^*, i_b^*, and i_c^* are represented compactly as i_{abc}^* and the three individual phase currents are represented as i_{abc}. Errors between the actual and commanded currents are fed to compensators, denoted G_C, which are ultimately used to generate the PWM gate signals. A variety of compensator types, as shown in [11], [12], could be implemented. Reactive power can be supplied or consumed by altering the phase angle of the current commands. The overall function of the control system is to increase the output current when $v_{pv} > v_{mpp}$ and decrease the output current when $v_{pv} < v_{mpp}$ where v_{mpp} is the voltage at the module maximum power point (MPP).

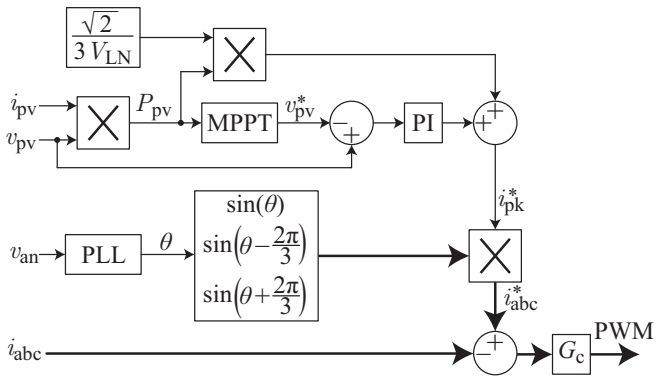

Figure 2. Inverter controller

IV. Cost

The cost of the three-phase VSI will be compared to a two-stage single-phase microinverter. Given that a microprocessor, sensing, EMI filtering, and packaging are common to most inverters, any difference in cost is likely to be associated with the power electronic circuit. To facilitate an objective comparison between passive component cost, it will be assumed that the price of capacitors and magnetic devices are linearly dependent on rated peak energy storage, E_C, and core volume, K_{vol}, respectively. Similarly, the power MOSFET price will be modeled to be linearly dependent on the kVA rating, K_{kVA} [13]. Thus, the cost of a capacitor, a ferrite core magnetic device, and MOSFET can be expressed as

$$\Gamma_C = 2.36\frac{\$}{\text{J}} \times E_C + \$1.14 \tag{2}$$

and

$$\Gamma_L = 0.00024\frac{\$}{\text{mm}^3} \times K_{vol} + \$0.66 \tag{3}$$

and

$$\Gamma_{MOS} = 0.384\frac{\$}{\text{kVA}} \times K_{kVA} + \$0.3 \tag{4}$$

respectively, where the coefficients were determined from linear regressions of the price data shown in the Appendix. The total power circuit cost is found by applying (2)–(4) to each inverter component and summing contributions.

A. Single-Phase Microinverter

First, the cost of the single-phase microinverter will be considered. It can be shown that the minimum required decoupling capacitance, $C_{1\phi}$, of a single-phase inverter with a high-voltage dc link can be expressed as

$$C_{1\phi} = \frac{P_{rated}}{4\pi f_{grid} V_{avg} \widetilde{v}} \tag{5}$$

where V_{avg} is the average dc-link voltage and $\widetilde{v}$ is the dc-link voltage ripple magnitude [6], [13]. Assuming a 250 W rating, a 60 Hz grid frequency, an average dc-link voltage of 400 V, and a ripple magnitude of 35 V, the minimum required capacitance is 23.7 μF. This relatively large capacitance is generally satisfied with several parallel film capacitors. Assuming n_C parallel capacitors are used, the rated peak energy stored in one decoupling capacitor is

$$E_{C(1\phi)} = \frac{1}{2}\frac{C_{1\phi}}{n_C}\left(1.5 \times V_{avg}\right)^2 \tag{6}$$

where 1.5 is a voltage derating factor. The total price of the decoupling stage is found by substituting (6) into (2) and evaluating n_C times. A single-phase microinverter typically requires an inductor in the input dc-dc converter, an isolation transformer, and output filter inductance. Given the effective core volume of a each component, (3) can be used to estimate the price of magnetics. Although several single-phase inverter topologies exist, it will be assumed that the microinverter

has two stages: an isolated boost converter at the input and an H-bridge at the output. Each stage has four MOSFETs. The total price of MOSFETS is found by evaluating the kVA rating of each component in (4) and summing. Diode costs are neglected. It will be assumed that the single-phase inverter is interfaced with a 240 V split-phase system.

B. Three-Phase Microinverter

The cost of the proposed 250 W three-phase microinverter will now be considered. Given an MEPV MPP voltage, v_{mpp}, of 400 V, a 200 nF input capacitance, and a 1.5 voltage derating factor, the rated peak energy stored in the dc link is only 36 mJ. In comparison to the single-phase microinverter, the capacitive energy storage requirement is reduced by more than two orders of magnitude. The single-stage, three-phase microinverter does not require an isolation transformer or input inductance. The associated price of the three output filter inductors and hex-bridge can be evaluated using (3) and (4), respectively.

C. Cost Comparison

The component quantities, ratings, and costs associated with the proposed three-phase and conventional single-phase microinverters are compared in Table II. Results indicate that the proposed three-phase inverter power circuit is approximately 60% lower in cost than the single-phase design. The cost breakdown demonstrates that the largest portion of cost savings in the three-phase inverter is associated with the large reduction in film capacitance requirements.

Table II
COMPONENT RATINGS AND COST COMPARISON OF PROPOSED THREE-PHASE INVERTER AND SINGLE-PHASE INVERTER

	proposed three-phase microinverter	single-phase microinverter
input inductor	—	$1 \times (4,370\,\text{mm}^3)$ ⇓ \$1.71 – 6%
transformer	—	$1 \times (4,370\,\text{mm}^3)$ ⇓ \$1.71 – 6%
dc-link capacitor(s)	$1 \times (200\,\text{nF} @ 600\,\text{V})$ ⇓ \$1.22 – 11%	$5 \times (5\,\mu\text{F} @ 600\,\text{V})$ ⇓ \$16.30 – 60%
MOSFETs	$6 \times (600\,\text{V},\ 1\,\text{A})$ ⇓ \$3.18 – 29%	$4 \times (60\,\text{V},\ 6.25\,\text{A})$ & $4 \times (600\,\text{V},\ 1.5\,\text{A})$ ⇓ \$4.36 – 16%
output inductor(s)	$3 \times (6,190\,\text{mm}^3)$ ⇓ \$6.44 – 59%	$1 \times (10,700\,\text{mm}^3)$ ⇓ \$3.23 – 12%
total price	\$10.8	\$27.3

V. EFFICIENCY

A. Loss Modeling

A dynamic simulation of the proposed three-phase circuit in Fig. 1 was prepared using PLECS. Gate driver and microprocessor power losses were calculated analytically while switching losses and core losses were estimated using datasheet parameters. The relative contributions of all losses will be accounted for and overall efficiency will be calculated. It will be shown that the presented circuit outperforms the most efficient single-phase microinverters and is competitive with leading multi-kW three-phase inverter designs on the PV market. Inverter efficiency with Si and SiC power MOSFETs will be compared.

Conduction and Core Losses: The modeled sources of conduction loss are the winding resistance, R_{W}, of each inductor and MOSFET on resistance, R_{DS}. Given that the 6 mH inductance is satisfied with a P36/22 pot core containing 155 turns of 24 AWG wire, the winding resistance was estimated as 0.9Ω [14]. A switching frequency of 50 kHz and the inductance value can be used to calculate the current ripple magnitude and estimate specific core loss as $10\,\text{kW/m}^3$ [15]. The total core loss of three inductors which each have an effective volume of $10{,}700\,\text{mm}^3$ is approximately $3 \times 10,700\,\text{mm}^3 \times 10\,\text{kW/m}^3$. Commercially available Si and SiC MOSFETs with parameters summarized in Table III were considered.

Table III
SI AND SIC MOSFET DATA

Material	Manufacturer	Part Number	R_{DS} [Ω]	V_{BR} [V]
Si	Infineon	IPA60R280C6	0.28	600
SiC	Cree	CMF20120D	0.08	1200

Gate Driver Losses: The gate driver can be modeled using the equivalent circuit in Fig. 3. The MOSFET, along with its junction capacitances, C_{gd} and C_{gs}, and intrinsic gate resistance, $R_{\text{G,I}}$, is enclosed in the dashed box. V_{DRV} must be sufficiently higher than the MOSFET threshold voltage for effective operation. Because SiC MOSFETs have a high threshold voltage and require a large drive voltage, V_{DRV} values of 10 V and 20 V were chosen for the Si and SiC circuits, respectively.

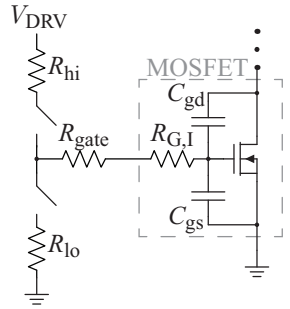

Figure 3. Gate-driver model

The total loss of all six gate drivers, P_{gates}, can be expressed analytically as

$$P_{\text{gates}} = 6\left(P_{\text{G}} + P_{\text{DRV(on)}} + P_{\text{DRV(off)}}\right) + P_{\text{DRV(IC)}} \qquad (7)$$

where P_{G} is the power dissipated due to periodic charging of the gate capacitance, $P_{\text{DRV(on)}}$ and $P_{\text{DRV(off)}}$ are the ohmic power dissipation during turn-on and turn-off, respectively, and $P_{\text{DRV(IC)}}$ is the quiescent power consumption of the driver

IC(s). P_{G} can be approximated as

$$P_{\mathrm{G}} = V_{\mathrm{DRV}} Q_{\mathrm{G}} f_{\mathrm{sw}} \tag{8}$$

where Q_{G} is the charge that must be transferred to and from the gate to initiate a switch transition. Q_{G}, as provided on the MOSFET datasheets, was 43 nC and 91 nC for the Si and SiC devices, respectively. $P_{\mathrm{DRV(on)}}$ and $P_{\mathrm{DRV(off)}}$ can be expressed [16] as

$$P_{\mathrm{DRV(on)}} = \frac{1}{2} \frac{R_{\mathrm{hi}} V_{\mathrm{DRV}} Q_{\mathrm{G}} f_{\mathrm{sw}}}{R_{\mathrm{hi}} + R_{\mathrm{gate}} + R_{\mathrm{G,I}}} \tag{9}$$

and

$$P_{\mathrm{DRV(off)}} = \frac{1}{2} \frac{R_{\mathrm{lo}} V_{\mathrm{DRV}} Q_{\mathrm{G}} f_{\mathrm{sw}}}{R_{\mathrm{lo}} + R_{\mathrm{gate}} + R_{\mathrm{G,I}}} \tag{10}$$

The parameters $R_{\mathrm{hi}} = 15\,\Omega$, $R_{\mathrm{lo}} = 5\,\Omega$, and $P_{\mathrm{DRV(IC)}}$ were taken from the gate driver IC datasheet [17]. R_{gate} was estimated as $2\,\Omega$.

Microprocessor Power Consumption: The inverter controller in Fig. 2 will be implemented using a microprocessor. A device from the Texas Instruments TMS320F280x will product line is used. As indicated the datasheet [18], the power consumption, P_{DSP}, of this type of microprocessor can be estimated as

$$P_{\mathrm{DSP}} = \left(\frac{0.41\ \mathrm{W}}{50\ \mathrm{MHz}} \right) f_{\mathrm{sysclkout}} + 0.22\,\mathrm{W} \tag{11}$$

where $f_{\mathrm{sysclkout}}$ is the clock frequency. It will be assumed that $f_{\mathrm{sysclkout}} = 50$ MHz.

B. Efficiency Simulation Results

The total loss in the inverter can be expressed as

$$P_{\mathrm{loss}} = P_{\mathrm{sw}} + P_{\mathrm{Rds}} + P_{\mathrm{Rw}} + P_{\mathrm{core}} + P_{\mathrm{DSP}} + P_{\mathrm{gates}} \tag{12}$$

where P_{sw} is the switching loss, P_{core} is the inductor core loss, and P_{Rds} and P_{Rw} are the semiconductor and inductor winding conduction losses, respectively. A weighted and peak efficiency will be presented for the proposed three-phase microinverter with both Si and SiC MOSFETs. The California Energy Commission uses a weighted efficiency:

$$\begin{aligned} \eta_{\mathrm{CEC}} = \ & 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + \\ & 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \end{aligned} \tag{13}$$

where $\eta_{10\%}$, $\eta_{20\%}$, ... is the efficiency when the inverter is operated at 10%, 20%, ... of rated power. The efficiency at each operating point is shown in Figs. 4(a) and 4(b) with gate-driver losses excluded and included, respectively. A comparison of the efficiency curves shows that gate-driver losses can be significant in the SiC inverter.

Using (13) and the data in Fig. 4(b), the CEC efficiency of the inverter with both Si and SiC MOSFETs is 97.7%. The relative contributions of each power loss type are summarized in Fig. 5. Results indicate that the gate driver losses are substantially larger in the SiC MOSFET inverter and that this adversely impacts power delivery at low-power operating conditions. This can be attributed to the larger Q_{G} value and V_{DRV} requirement of the commercially available SiC MOSFET used in this example. Semiconductor conduction losses are relatively small in both designs, but switching losses are higher with Si MOSFETs.

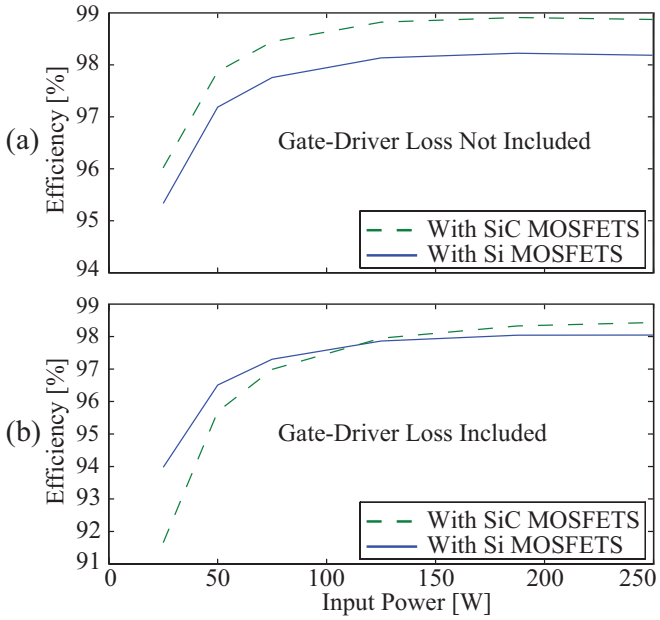

Figure 4. Inverter efficiency at various operating points; (a) Without gate-driver loss; (b) With gate-driver losses

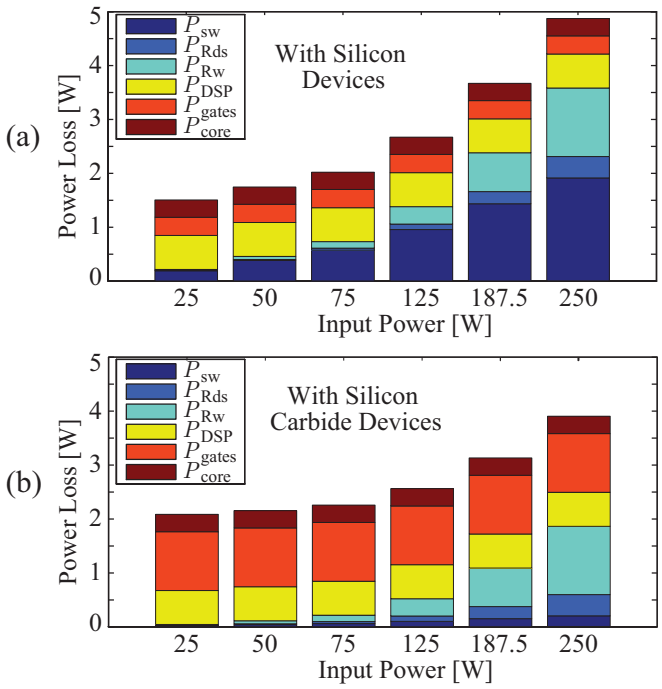

Figure 5. Loss contributions at various operating points; (a) Inverter with Si MOSFETs; (b) Inverter with SiC MOSFETs

Efficiencies of the proposed inverter, the three-phase CSI presented in [7], and several of the most highly efficient commercially available inverters are compared in Table IV. Given that modules typically have $\pm 3\%$ variation in power

output [19], [20], mismatch losses in series connected modules will be accounted for by introducing a net CEC efficiency, η_{net}, value in Table IV. Assuming mismatch losses average 1.5%, η_{net} is calculated by penalizing the nameplate CEC efficiency of centralized inverters with series modules. Results indicate that the proposed inverter is likely to be much more efficient than available single-phase microinverters and closely rivals high-performance three-phase inverters.

Table IV
EFFICIENCY COMPARISON BETWEEN INVERTERS [21]

manufacturer and model	ratings	η_{peak}	η_{CEC}	η_{net}
Proposed Inverter: Si	250 W, 3ϕ, 208V	**98.0**	**97.7**	**97.7**
Proposed Inverter: SiC	250 W, 3ϕ, 208V	**98.4**	**97.7**	**97.7**
CSI Inverter in [7]	200 W, 3ϕ, 400V	97.0	96.0	96.0
SMA: SB8000TL	8 kW, 3ϕ, 208V	99.0	98.0	96.5
Eaton: PV238	3.7 kW, 3ϕ, 208V	97.7	97.0	95.5
Enphase: M215x	215 W, 1ϕ, 240V	96.3	96.0	96.0
SolarBridge: P235x	215 W, 1ϕ, 235V	95.5	94.5	94.5
Petra Solar: SunWave	200 W, 1ϕ, 120V	95	93.0	93.0

VI. RELIABILITY

In this section, the reliability of the proposed inverter will be analyzed. The circuit components will be modeled as series-connected function blocks. The series topology does not correspond to the physical interconnections of the circuit and is intended to show that a failure of any one component will cause a system failure. Function blocks will represent various components in the power circuit.

System failure can be described using a probability density function (pdf), written as $f(t)$. The cumulative density function (cdf) represents the probability that a failure occurred at or before time t and can be expressed as

$$F(t) = \int_0^t f(\tau)\, d\tau \tag{14}$$

where $\lim_{t\to\infty} F(t) = 1$. The reliability function is defined as

$$R(t) = 1 - F(t) \tag{15}$$

and the net failure rate of the system is

$$\lambda_{\text{net}}(t) = \frac{f(t)}{R(t)} \tag{16}$$

In a series-connected system model, λ_{net} is the sum of the individual component failure rates. The mean time to failure (MTTF) of the system [22] is

$$\text{MTTF} = \int_0^\infty R(t)\, dt \tag{17}$$

In the following analysis, repairs will not be considered. It will be assumed that all device failure rates are constant [22] such that

$$f(t) = \lambda_{\text{net}} e^{-\lambda_{\text{net}} t} \tag{18}$$

and

$$\text{MTTF} = \int_0^\infty e^{-\lambda_{\text{net}} t} dt = \frac{1}{\lambda_{\text{net}}} \tag{19}$$

A. Calculation of Failure Rates

The component failure rates must be determined before MTTF can be calculated. The most widely used data comes from the military handbook MIL-HDBK-217F. Generally, the failure rates predicted in MIL-HDBK-217F are regarded as pessimistic. A device failure rate is expressed as

$$\lambda = \lambda_{\text{b}} \prod_{j=1}^{n} \pi_j \tag{20}$$

where λ_{b} is the base failure rate and the π_j factors are dependent on operating conditions. Generally, there is a temperature-dependent modifying factor, in addition to others which depend on device ratings and circuit stresses [23].

1) Capacitors: The failure rate of a capacitor, λ_{C}, is modeled

$$\lambda_{\text{C}} = \lambda_{\text{b}} \pi_{\text{T}} \pi_{\text{C}} \pi_{\text{V}} \pi_{\text{Q}} \pi_{\text{E}} \tag{21}$$

where π_{T} is the temperature factor, π_{C} is a capacitance dependent factor, π_{V} is a voltage stress factor, π_{Q} is the quality factor, and π_{E} is the environment factor. Highly reliable film capacitors will be utilized in the design.

2) Inductors: The inductor failure rate, λ_{L}, is of the form

$$\lambda_{\text{L}} = \lambda_{\text{b}} \pi_{\text{T}} \pi_{\text{Q}} \pi_{\text{E}} \tag{22}$$

3) Power MOSFETs: Considering that power MOSFETs have evolved considerably since MIL-HDBK-217F was published, currently available manufacturer data will be used instead. ON Semiconductor has a database of MTTF data for currently available products. A component with the required design ratings will be selected from this database and used to estimate the lifetime of the inverter MOSFETs. Since field data of SiC MOSFET reliability is limited, it will be assumed that Si and SiC MOSFET failure rates are equal.

4) Overall Failure Rate: Using the above equations, the net failure rate is

$$\lambda_{\text{net}} = \lambda_{\text{C}} + 3\lambda_{\text{L}} + 6\lambda_{\text{MOS}} \tag{23}$$

The coefficients in (23) are equal to the number of corresponding components in the circuit.

B. Reliability Results

The calculated failure rates and MTTFs of the inductors and capacitor at an ambient temperature of 80 °C are shown in Table V. The ON Semiconductor MOSFET with part number MTB2P50E has a MTTF of 113,714,796 hrs when the junction temperature is 80 °C [24]. The MOSFET hex-bridge failure rate in Table V is equal to $6\frac{1\times10^6}{113,714,796}$ failures per 10^6 hours. As the failure rate of the capacitor and three inductors is at least an order of magnitude smaller than that of the six MOSFETs, it can be concluded that the MTTF of the MOSFETs and the overall system are essentially equal. Multiplying the

Table V
FAILURE RATES AND MTTF OF EACH COMPONENT TYPE AT 80°C

	failures per 10^6 hours	MTTF [years]
MOSFET hex-bridge	52.8×10^{-3}	2,160
Capacitor	3.01×10^{-3}	37,700
Inductors	526×10^{-6}	216,000
Overall	56.3×10^{-3}	2,030

overall failure rate in Table V by 1×10^6 and converting units, it can be shown that approximately 500 out of 1 million units can be expected to fail annually.

The analysis shows that the proposed design is highly reliable and can be expected to have a lifetime on par with a typical module. The results also indicate that the MOSFETs are the components most likely to fail. Given that MOSFET failure rate is highly dependent on temperature, this implies that design efforts should be highly targeted towards thermal management.

VII. Experimental Results

A prototype of the circuit in Fig. 1 is shown in Fig. 6. The inverter was configured to deliver power from a 350 V dc power supply to a three-phase 100 Ω load. Results in Fig. 7 confirm that sinusoidal output current was successfully injected into a load.

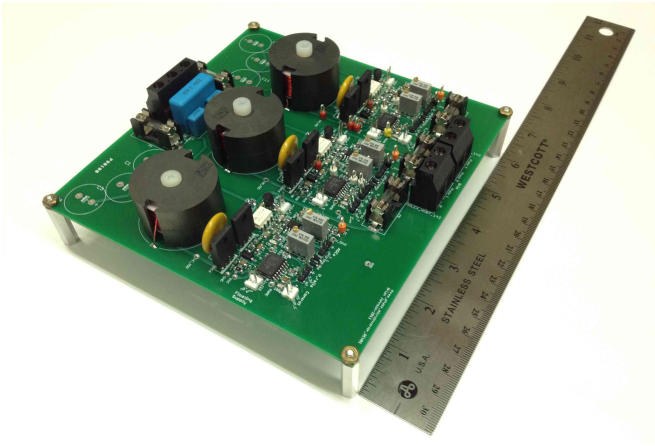

Figure 6. 250 W three-phase microinverter prototype

VIII. Conclusion

A single-stage, three-phase voltage source inverter compatible with a micro-systems enabled PV and micro-transfer printed PV has been introduced. The high-voltage capabilities of these PV technologies can be leveraged to formulate an extremely simple inverter design which substantially reduces the number of circuit components. Benefits of fewer components include low cost, high reliability, and high efficiency. It has been shown that the proposed design has a peak expected efficiency at or above 98%. This performance exceeds the most efficient single-phase microinverters and is competitive with leading multi-kW three-phase inverter designs. Furthermore,

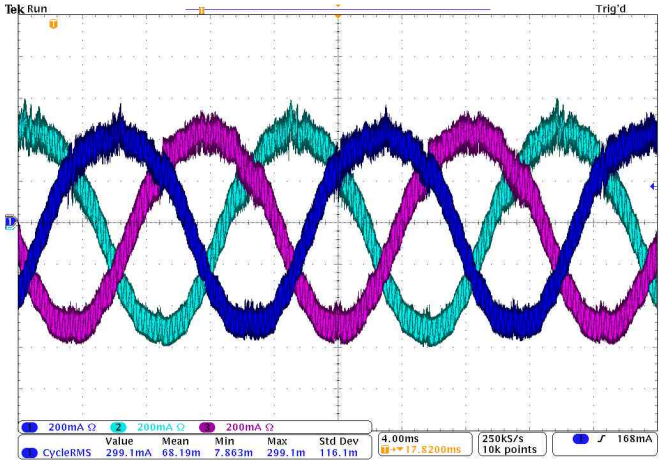

Figure 7. Output current of prototype

analysis indicates that costs can be reduced by approximately 60% in comparison to a conventional single-phase design. Experimental results were presented. In summary, the design under consideration simultaneously achieves high efficiency, long life, and low cost. Future work will be focused on grid-connected operation and detailed experimental validation.

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Appendix

The linear regression and cost data for film capacitors, ferrite cores, and power MOSFETs are summarized below.

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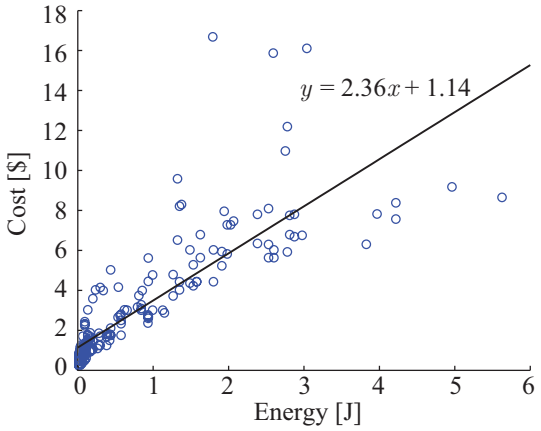

Figure 8. Capacitor cost data and best-fit line

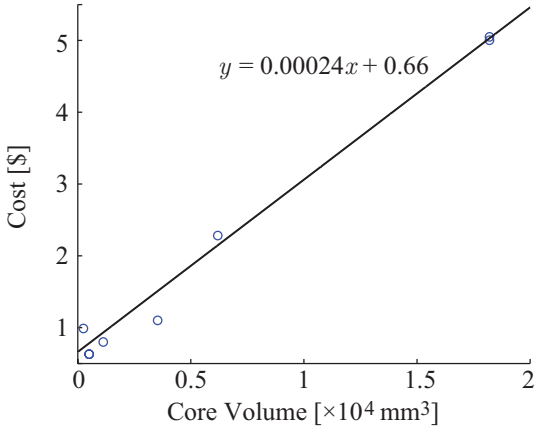

Figure 9. Ferrite core cost data and best-fit line

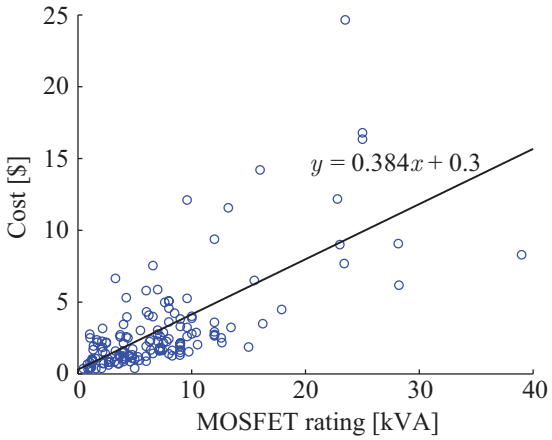

Figure 10. MOSFET cost data and best-fit line

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