Decentralized Carrier Phase Shifting for Optimal Harmonic Minimization in Asymmetric Parallel-Connected Inverters

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***Abstract*—This article presents a carrier phase shifting technique for minimizing the aggregate harmonics in networks of asymmetric parallel-connected inverters for distributed power generation system applications. The proposed technique is: 1) implemented in a *decentralized* manner, relying only on local voltage and current measurements, and 2) *optimal* in the sense that it minimizes a cost function representing the carrier-frequency current harmonics. The analysis indicates that the proposed optimal carrier phase shifting technique can enable order-of-magnitude reductions in harmonic power, and also universal improvements compared to symmetric carrier interleaving for asymmetric inverter networks. Moreover, compared to existing methods that require either centralized communication or information exchange between inverters to coordinate carriers, the proposed technique is completely decentralized, which provides important practical benefits for implementation, including improved robustness and reduced cost. The technique is experimentally validated on a network of three single-phase 2-kW inverters and demonstrates a 36.5% reduction in the weighted total harmonic distortion factor of the aggregate inverter current, and the ability to converge to the optimal carrier phase spacing dynamically in less than one line frequency cycle (16.7 ms) in steady state and transient operating conditions.**

***Index Terms*—DC–AC power converters, harmonic distortion, optimization methods, power conversion harmonics.**

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I. Introduction

DISTRIBUTED power generation systems are becoming increasingly important in integrating significant quantities of renewable energy and storage with the bulk electric grid [1], [2]. In such systems, multiple distributed input or output parallel-connected voltage source inverters are connected to a single point-of-common-coupling (PCC) at the distribution or transmission level. Variations and asymmetries among the distributed energy sources and inverters can result in aggregate harmonic spectra at the PCC that are poorly characterized and are higher than expected due to constructive harmonic inference. Such scenarios can originate from the operating dynamics of the system—for instance, a collection of residential grid-connected photovoltaic inverters can exhibit variations in input voltages due to uneven irradiation or partial shading. Similarly, these scenarios can arise from variations in the inverter or system hardware—for instance, passive filter components in battery energy storage inverters can have upwards of fifty percent tolerances while also changing as a function of operating point and temperature (see, e.g., [3]–[5]). Analyzing these asymmetries is important since such variations are common in many practical settings and also impact the aggregate harmonic content. Standards such as IEEE 519-2014 [6] dictate the total harmonic distortion (THD) that is allowable at the PCC of such systems with the electric grid. High-order electromagnetic interference (EMI) filters or active power filters can possibly be utilized to meet such standards, but they naturally tend to add to the cost, complexity, and volume of the overall system.

Various carrier phase shifting and interleaving techniques have been proposed as a control-based alternative to minimize harmonics, mostly in nondistributed series- or parallel-connected inverter applications. In reviewing these existing works, we first identify two important characteristics that are particularly relevant to distributed inverter systems. First, we desire an *optimal* strategy that will yield the carrier phase spacing that results in the lowest possible aggregate harmonic spectra across all possible component and operating asymmetries. Second, we desire a *decentralized* strategy that requires no communication between individual inverters. Particularly in a distributed setting, the use of centralized communication, even for 'slow' variables or commands, can be cost-prohibitive, reduce system reliability and robustness, and preclude applications where communication or centralization are not viable options.

Symmetric carrier interleaving, whereby, the carriers of N inverters are evenly spaced $360^\circ/N$ over a switching period, has been applied to applications including grid-connected pulsewidth modulation (PWM) rectifiers [7], flying capacitor multilevel inverters for aircraft electrification [8], shunt active power filters for grid power conditioning [9], and Z-source inverters [10]. Recent works have also demonstrated fully decentralized approaches for achieving symmetric carrier interleaving [11]. However, if the inverter network is asymmetric, as in the scenarios discussed above, symmetric interleaving does not optimally minimize the aggregate voltage or current harmonics. Additionally, as will be demonstrated in this article, while symmetric interleaving can yield some reduction in carrier frequency harmonics for asymmetric networks, its effectiveness is greatly diminished as the magnitudes of the asymmetries increase. Other works have explored improving upon the optimality of symmetric carrier interleaving. In [12] and [13], the authors analyze regular asymmetric interleaving, whereby the carriers of N inverters are evenly spaced but are not restricted to be $360^\circ/N$. By utilizing this technique, the aggregate harmonics can be shaped according to a particular EMI specification. The technique improves upon the harmonic reduction capability of symmetric interleaving, but it is not necessarily optimal given the constraint that the carriers must be evenly spaced.

Optimal carrier phase spacing techniques that minimize a particular cost function have also been presented in prior works. In [14], the authors propose a method for computing the optimal interleaving angle of two paralleled inverters based on the real and reactive power, dc link voltage, and average modulation index. In [15], the authors present an optimal carrier phase spacing strategy for paralleled multilevel converters in order to reduce magnetic fluxes and associated losses. In [16], the authors propose a carrier synchronization method that utilizes particle swarm optimization to compute the optimal carrier phase spacing, albeit with global information including the dc-link voltage and output power of each inverter. In [17], the authors present a strategy for minimizing the first carrier frequency harmonic in networks of asymmetric dc-dc converters. All of these techniques are centralized in the sense that they require an omniscient controller that can compute the optimal phase spacing based on global variables. Moreover, some techniques (e.g., the ones in [14], [15], and [17]) require a centralized controller that distributes PWM signals to every inverter; this can be a prohibitive constraint for distributed applications in which sending high frequency PWM signals to physically separated inverters could be largely impractical.

To the best of the authors' knowledge, existing methods are limited in that they either do not yield the optimal carrier phase spacing (as is the case with symmetric interleaving) or require the use of centralized communication, which limits the applicability for distributed inverter networks. To address these limitations, this work presents a carrier phase shifting strategy for asymmetric single-phase inverter networks that can simultaneously enable decentralized and optimal minimization of undesired aggregate carrier-frequency harmonics. The proposed strategy utilizes a decentralized optimization method that is implemented on each inverter with voltage and current measurements that are measured locally. Since no communication is required between the inverters, the approach is completely decentralized unlike existing literature and presents obvious benefits with regards to scalability, modularity, and fault tolerance.

In this article, we present the design of the proposed decentralized optimization method and an analysis of its performance and optimality in minimizing aggregate current harmonics. The analysis indicates that the proposed optimal carrier phase shifting strategy can enable order-of-magnitude improvements in distortion power compared to the worst-case carrier phase shifting (when carrier frequency harmonics constructively sum) for certain asymmetric inverter networks. Moreover, the proposed technique offers universal improvement over symmetric carrier interleaving for any asymmetries that arise in such networks. The technique is experimentally implemented on a network of three 2-kW inverters and demonstrates a 36.5% improvement in the weighted total harmonic distortion (WTHD) factor at the PCC.

Conceptually, the idea of an optimization-driven approach for minimizing aggregate harmonics of distributed interconnected power converters has been developed by the authors for networks of dc-dc converters that are connected in parallel or series at the input or output, e.g., point-of-load converters or dc microgrids [18], [19]. We termed this method broadly as *minimum distortion point tracking*. Thus, while the algorithmic details and optimization method presented in this article are tailored to parallel-connected single-phase inverters, the concept is generalizable and can be applied, in theory, to arbitrary networks of interconnected power converters. Indeed, design and analysis techniques beyond the ones presented in this article can be utilized to analyze larger and more general networks of inverters, for instance, three-phase inverters or inverters that are connected in series or parallel at the input or output.

The remainder of this article is organized as follows. Section II quantifies the aggregate harmonics in networks of parallel-connected inverters for various asymmetries, including nonuniform input voltages and variations in passive component parameters. Additionally, we analyze the limits of the maximum harmonic reduction possible with carrier phase shifting and the achievable improvement in harmonic reduction compared to symmetric carrier interleaving. Section III presents the decentralized carrier phase shifting algorithm for attaining the maximum achievable reduction of aggregate harmonics based on locally sensed voltage and current measurements, along with a SPICE-based numerical simulation validation. Section IV presents experimental results that validate the proposed method on a network of three output-parallel connected single-phase 2-kW inverters. Section V discusses the impact of nonidealities and other practical implementation considerations, including a verification of the algorithm performance in the presence of nonnegligible line impedances that can be present in physically distributed inverter networks. Finally, Section VI concludes the article and provides a few directions for future work.

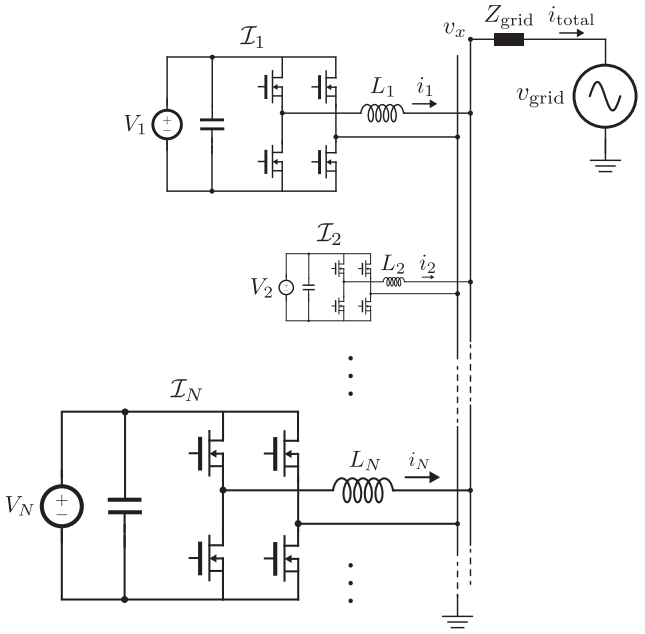


Fig. 1. Network of N nonidentical single-phase inverters $\mathcal{I}_1, \ldots, \mathcal{I}_N$ connected in parallel to a voltage source v_{grid} through an impedance Z_{grid}. The inverters can have unique input voltages $V_1, \ldots, V_N$ and output inductances $L_1, \ldots, L_N$, as is common in distributed power generation systems with multiple parallel-connected voltage source inverters connected to a single PCC. A common carrier frequency ω_c is assumed.

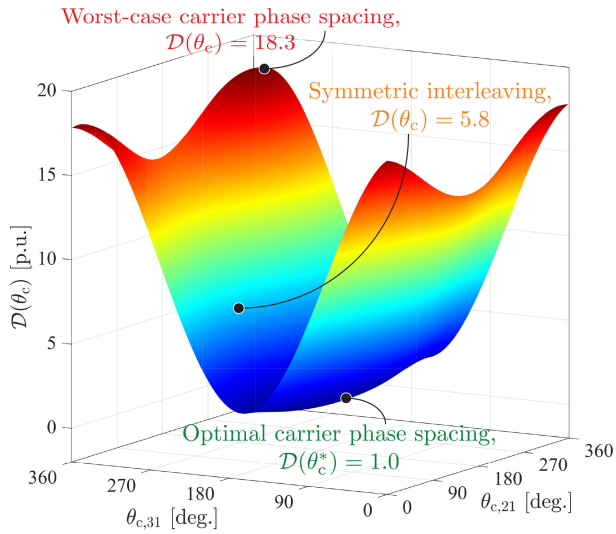


Fig. 2. Distortion $\mathcal{D}(\theta_c)$ plotted as a function of the carrier phase spacing θ_c for an asymmetric network of three output parallel-connected inverters with nonidentical input voltages and output inductances. As shown, the optimal carrier phase spacing $\theta_c^\star$ enables a $5.8\times$ reduction in distortion compared to symmetric carrier interleaving and a $18.3\times$ reduction compared to the worst-case carrier phase spacing.

II. Harmonic Analysis and Carrier Phase Shifting for Asymmetric Inverter Networks

In this section, we will analyze the effect of carrier phase shifting on aggregate harmonics in networks of asymmetric parallel-connected inverters. First, we will derive a closed-form analytical expression for the aggregate distortion as a function of the carrier phase spacing across N asymmetric single-phase inverters. This expression utilizes well-known harmonic models that are found in the literature. Then, we will analyze how the magnitude of distortion varies as a function of: 1) the carrier phase spacing and 2) asymmetries that manifest in the inverter network, namely, variations in the input voltages and variations in the inverters' filter parameters. The results of this section will show that: 1) network asymmetries can cause increased distortion that cannot be adequately addressed with symmetric carrier interleaving, and 2) the optimal carrier phase spacing can provide significant reductions in distortion, particularly in the presence of such asymmetries.

A. Modeling Distortion in Asymmetric Inverter Networks

Consider N single-phase inverters $\mathcal{I}_1, \ldots, \mathcal{I}_N$ with independent dc voltage inputs $V_1, \ldots, V_N$ connected in parallel on the ac side to an ideal voltage source v_{grid} through an impedance Z_{grid}. Fig. 1 illustrates the architecture. The time-domain analytical harmonic solution for the output current of a single-phase inverter with a double-edge naturally sampled PWM is derived in [20]. In the context of Fig. 1, this allows us to express the output current i_ℓ of the inverter $\mathcal{I}_\ell$ as follows:

$$i_\ell(t, \theta_{c,\ell}) = \frac{1}{\omega_0 L_\ell}\Big(v_x(t) - \big(2V_\ell M \cos(\omega_0 t) + \frac{8V_\ell}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos((m+n-1)\pi) \times \cos(2m(\omega_c t + \theta_{c,\ell}) + (2n-1)\omega_0 t)\big)\Big) \quad (1)$$

where $M \subset (0,1)$ is the modulation index, $J_n(\cdot)$ is a Bessel function of order n, ω_0 is the line frequency, ω_c is the carrier frequency, and $\theta_{c,\ell}$ is the carrier phase shift of $\mathcal{I}_\ell$. Although this expression is derived for a simple L filter at the inverter output, it can be easily modified to incorporate other filter configurations (e.g., LCL). We are interested in the harmonic components associated with the carrier frequency ω_c. These are denoted collectively by $\widetilde{i}_\ell(t, \theta_{c,\ell})$, and from (1), we see that they are given by

$$\widetilde{i}_\ell(t, \theta_{c,\ell}) = \frac{1}{\omega_0 L_\ell}\left(v_x(t) - \left(\frac{8V_\ell}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} \times \frac{1}{2m}J_{2n-1}(m\pi M)\cos((m+n-1)\pi) \times \cos(2m(\omega_c t + \theta_{c,\ell}) + (2n-1)\omega_0 t)\right)\right). \quad (2)$$

In both (1) and (2), we explicitly parametrize the currents with respect to the carrier angles since these will be optimization variables in subsequent developments. Collect the carrier phase shift of all inverters in a single vector $\theta_c := [\theta_{c,1}, \ldots, \theta_{c,N}]^{\mathrm{T}}$. Also note that from basic circuit laws, it is clear that $\widetilde{i}_1(t, \theta_{c,1}) + \cdots + \widetilde{i}_N(t, \theta_{c,N}) =: \widetilde{i}_{\text{total}}(t, \theta_c)$. With these preliminaries in

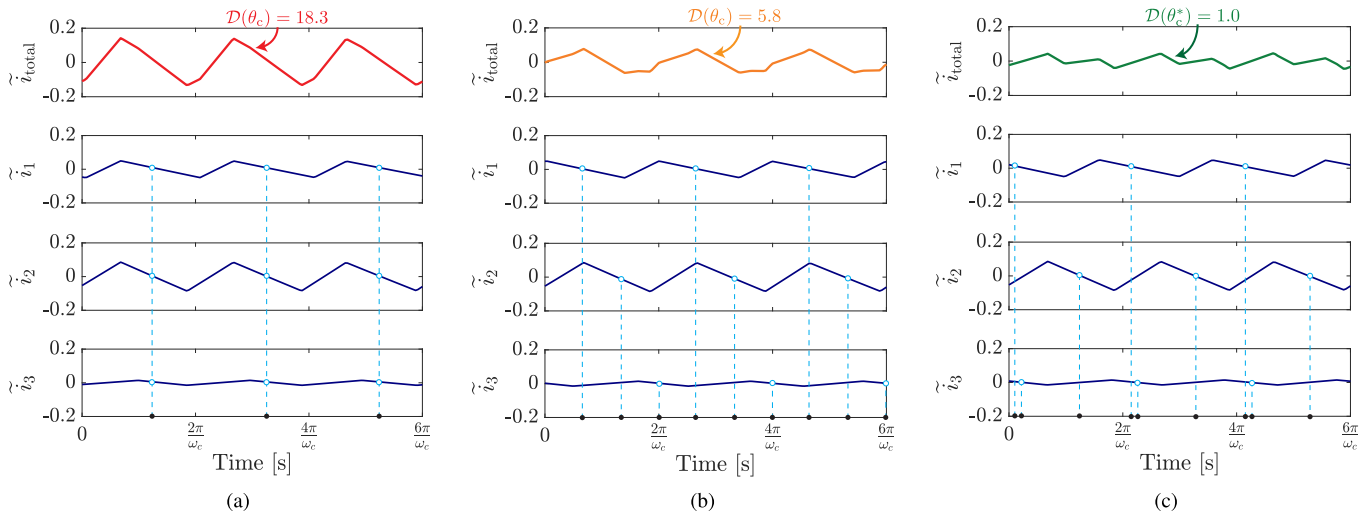


Fig. 3. Comparison of the carrier frequency (ω_c) components of the aggregate inverter current $\widetilde{i}_{\text{total}}$ and the individual inverter currents $\widetilde{i}_\ell$ for three carrier phase spacing scenarios in an asymmetric network of three parallel-connected inverters. (a) The worst-case carrier phase spacing yields a maximum peak-to-peak ripple of 0.29 p.u. and $\mathcal{D}(\theta_c) = 18.3$. (b) The symmetric interleaved carrier phase spacing yields a maximum peak-to-peak ripple of 0.17 p.u. and $\mathcal{D}(\theta_c) = 5.8$. (c) The optimal carrier phase spacing $\theta_c^\star$ yields a maximum peak-to-peak ripple of 0.08 p.u. and $\mathcal{D}(\theta_c) = 1.0$.

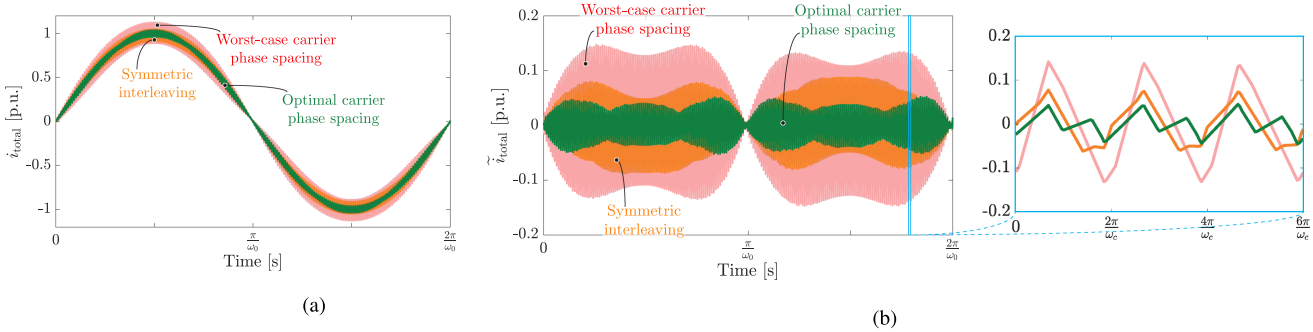


Fig. 4. Time domain comparison of the aggregate inverter current i_{total} between the worst-case carrier phase spacing (light red), symmetric interleaved carrier phase spacing (orange), and the optimal carrier phase spacing $\theta_c^\star$ (green). (a) Fundamental waveform for one ω_0 period. (b) The carrier frequency component of the aggregate current $\widetilde{i}_{\text{total}}$.

place, we define *distortion*, $\mathcal{D}$, to be the squared $\mathcal{L}_2$-norm of $\widetilde{i}_{\text{total}}(t, \theta_c)$

$$\mathcal{D}(\theta_c) := \left|\widetilde{i}_{\text{total}}(t, \theta_c)\right|_{\mathcal{L}_2}^2 = \int_0^{\frac{2\pi}{\omega_0}} \left|\widetilde{i}_{\text{total}}(\tau, \theta_c)\right|^2 d\tau. \quad (3)$$

This quantity quantifies the total carrier-frequency harmonics. Furthermore, it is closely related to the WTHD factor [20] (the only difference being a normalization factor).

B. Distortion as a Function of Carrier Phase Spacing

We will consider how $\mathcal{D}(\theta_c)$ varies as a function of θ_c for an asymmetric network of three output parallel-connected inverters, as shown in Fig. 1 for $N = 3$. We design the network of inverters such that there are asymmetries in both the input dc link voltages and the output inductances of every inverter. The dc link voltages are simulated with 50% variation such that $V_1 = 1.5$ p.u., $V_2 = 1.0$ p.u., and $V_3 = 2.0$ p.u., normalized to the amplitude of the grid voltage v_{grid}. Similarly, the output inductances of each inverter have a 50% variation such that $L_1 = 2.0$ p.u., $L_2 = 1.5$ p.u., and $L_3 = 1.0$ p.u., normalized to an arbitrary constant L_{nominal}.

Fig. 2 illustrates how $\mathcal{D}(\theta_c)$ varies for every possible carrier phase spacing θ_c. The surface exhibits a minimum at which point $\mathcal{D}(\theta_c)$ is minimized. We denote the carrier phase spacing that yields this optimal minimization of $\mathcal{D}(\theta_c)$ to be $\theta_c^\star$.[1] More precisely, we define

$$\theta_c^\star = \arg\min_{\theta_c} \mathcal{D}(\theta_c). \quad (4)$$

Conversely, at the worst-case phase spacing, when the carriers are synchronized at $\theta_c = [0°, 0°, 0°]^{\text{T}}$, $\mathcal{D}(\theta_c)$ is 18.3× higher than $\mathcal{D}(\theta_c)$ obtained at $\theta_c^\star$. This implies that a significant reduction in carrier harmonic distortion can be achieved with

[1] In general, $\mathcal{D}(\theta_c)$ is not necessarily a convex function, and therefore multiple minima, and thus, multiple $\theta_c^\star$, can exist. However, in related work [18], we have demonstrated that the value of $\mathcal{D}(\theta_c)$ obtained at local minima are relatively similar.

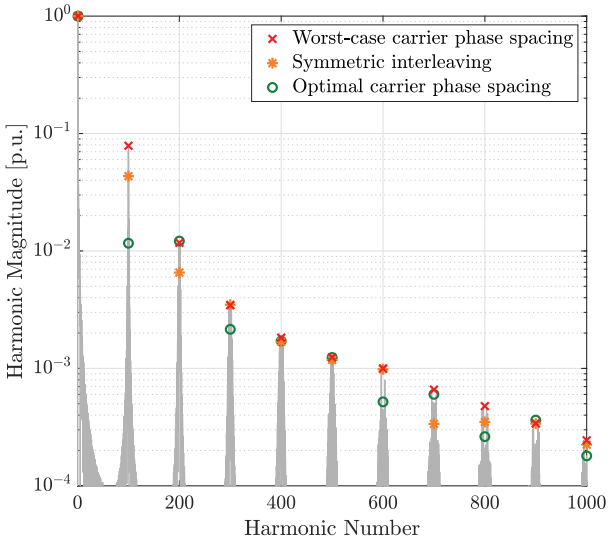


Fig. 5. Frequency domain comparison of the aggregate inverter current i_{total} between the worst-case carrier phase spacing, symmetric interleaved carrier phase spacing, and the optimal carrier phase spacing; $\omega_c/\omega_0 = 100$.

optimal carrier phase shifting. As a point of comparison with state-of-the-art methods, symmetrically interleaving the carriers, i.e., setting $\theta_c = [0°, 120°, 240°]^T$, results in $\mathcal{D}(\theta_c)$ being $5.8\times$ higher. Thus, while symmetric interleaving is a simple and open-loop technique that can reduce $\mathcal{D}(\theta_c)$ from the worst-case scenario, there is still a substantial reduction in distortion that can be achieved with an optimal carrier phase shifting strategy.

The impact of θ_c on $\mathcal{D}(\theta_c)$ can be further studied with time domain representations of the relevant current waveforms. Fig. 3 illustrates the carrier frequency dynamics from the inverter network for each of the three aforementioned carrier phase spacings: 1) the worst-case carrier phase spacing $\theta_c = [0°, 0°, 0°]^T$; 2) the symmetrically interleaved carrier phase spacing $\theta_c = [0°, 120°, 240°]^T$; and 3) the phase spacing $\theta_c^\star$ that optimally minimizes $\mathcal{D}(\theta_c)$. The worst-case carrier phase spacing [Fig. 3(a)] yields a maximum peak-to-peak ripple 0.29 p.u. due to the in-phase carrier components that constructively sum to increase the peak-to-peak magnitude of $\widetilde{i}_{\text{total}}(t, \theta_c)$. The symmetrically interleaved carrier phase spacing [Fig. 3(b)] yields a maximum peak-to-peak ripple of 0.17 p.u. since some components of the individual inverter currents, primarily $\widetilde{i}_1(t, \theta_c)$ and $\widetilde{i}_2(t, \theta_c)$, are partially in-phase. Finally, the optimal carrier phase spacing [Fig. 3(c)] yields a maximum peak-to-peak ripple of 0.08 p.u. since the carrier frequency components of the individual inverter currents are phase shifted in a way that minimizes the aggregate ripple. Namely, we see that $\widetilde{i}_1(t, \theta_c)$ and $\widetilde{i}_2(t, \theta_c)$ are phase shifted nearly 180° apart, while $\widetilde{i}_3(t, \theta_c)$ is phase shifted to compensate for the asymmetric shape of the carrier waveforms.

Fig. 4 illustrates the aggregate current waveform over a fundamental period $(1/\omega_0)$. Again, we see that the optimal carrier phase spacing visibly reduces the switching frequency ripple $\widetilde{i}_{\text{total}}(t, \theta_c)$, and, in particular, can offer better distortion minimization than symmetric interleaving. Fig. 5 shows a frequency domain analysis that provides further insight into the impact of

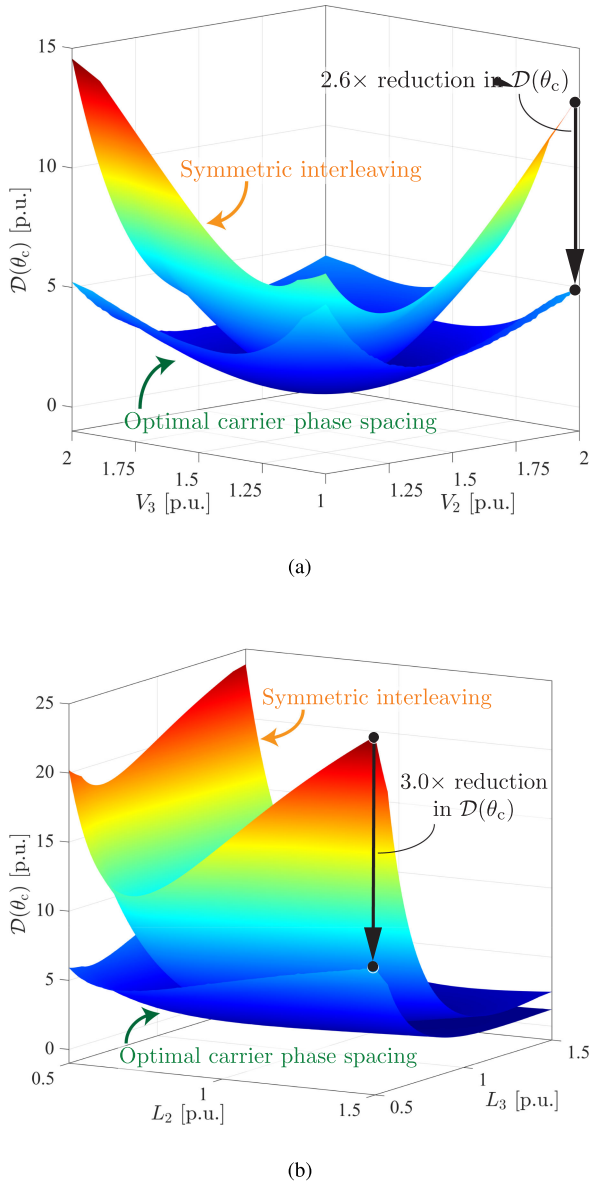


Fig. 6. Distortion $\mathcal{D}(\theta_c)$ plotted as a function of asymmetries in the (a) inverter input voltages and (b) inverter output inductances. (a) Asymmetries in the inverter input voltages can result in higher distortion $\mathcal{D}(\theta_c)$ even when using symmetric carrier interleaving. The optimal carrier phase spacing $\theta_c^\star$ can enable a $2.6\times$ reduction in distortion compared to symmetric carrier interleaving for this scenario. (b) Similarly, asymmetries in the inverter output inductances can result in higher distortion $\mathcal{D}(\theta_c)$. The optimal carrier phase spacing $\theta_c^\star$ can enable a $3.0\times$ reduction in distortion compared to symmetric carrier interleaving for this scenario.

carrier phase spacing on the harmonic content of the aggregate current. The optimal carrier phase spacing substantially reduces the harmonic magnitude of the first carrier frequency harmonic, along with further minimizations of multiple higher frequency harmonics. In contrast, symmetric interleaving provides only partial minimization of the first and second carrier frequency harmonic. It is important to note that carrier phase shifting can reduce the *total* harmonic power through destructive harmonic interference, and not simply spread existing harmonics across more frequencies or push them to higher harmonic frequencies,

as is characteristic of some existing works on programmed PWM techniques (e.g., [21], [22]).

C. Distortion as a Function of Network Asymmetries

Asymmetries in inverter networks can also manifest from operational characteristics (e.g., unequal input voltages $V_1, \ldots, V_N$) or from nonuniformities in passive and active components (e.g., variations in inverter output inductances $L_1, \ldots, L_N$). Here, we will consider how $\mathcal{D}(\theta_c)$ varies as a function of such asymmetries. In particular, we will quantify the achievable reduction in $\mathcal{D}(\theta_c)$ that is possible when using the optimal carrier phase spacing $\theta_c^\star$ compared to the symmetrically interleaved carrier phase spacing.

Again, we consider a network of three output parallel-connected inverters, as shown in Fig. 1, for $N = 3$. Fig. 6(a) illustrates how $\mathcal{D}(\theta_c)$ varies as a function of asymmetries in the input voltages. The voltages V_2 and V_3 are swept between 1.0 and 2.0 p.u., while V_1 is fixed at 1.5 p.u. As shown, the optimal carrier phase spacing $\theta_c^\star$ results in $\mathcal{D}(\theta_c)$ that is lower at every point compared to the symmetrically interleaved carrier phase spacing. When the asymmetry is greatest, that is, when $V_1 = 1.5$ p.u., $V_2 = 1.0$ p.u., and $V_3 = 2.0$ p.u., $\mathcal{D}(\theta_c)$ is $2.6\times$ lower at the optimal carrier phase spacing.

Next, Fig. 6(b) illustrates how $\mathcal{D}(\theta_c)$ varies as a function of asymmetries in the output inductances. The inductances L_2 and L_3 are swept between 0.5 and 1.5 p.u., while L_1 is fixed at 1.0 p.u. We see that the optimal carrier phase spacing minimizes $\mathcal{D}(\theta_c)$ across the entire region. At the worst point, $\theta_c^\star$ enables a $3.0\times$ reduction in distortion compared to symmetric carrier interleaving.

III. Decentralized Carrier Phase Shifting Algorithm for Optimal Harmonic Minimization

In this section, we present the decentralized carrier phase shifting algorithm that dynamically seeks the optimal carrier phase spacing $\theta_c^\star$. We emphasize the decentralized nature of the algorithm, that is, the optimization can be implemented locally for each inverter and does not require global knowledge of parameters or communication between inverters.

A. Algorithm Design

The objective of the algorithm from a global perspective is to determine the optimal carrier phase spacing $\theta_c^\star$ that minimizes $\mathcal{D}(\theta_c)$, that is, to solve the minimization problem posed in (4). Since the implementation is desired to be decentralized, the only control (decision) variable that is assumed to be available to the ℓth inverter is its carrier phase shift $\theta_{c,\ell}$. We utilize an iterative gradient method to update $\theta_{c,\ell}$ of each inverter [23]. Starting with the qth iteration, $\theta_{c,\ell}[q+1]$ is computed according to

$$\theta_{c,\ell}[q+1] = \theta_{c,\ell}[q] - \kappa \nabla_\ell \mathcal{D}(\theta_c[q]) \tag{5}$$

where κ is a positive scalar that is selected to tradeoff between numerical stability and convergence speed, and $\nabla_\ell \mathcal{D}(\theta_c[q])$ is the gradient of $\mathcal{D}$ with respect to $\theta_{c,\ell}$ at the qth iteration. This gradient can be computed as

$$\begin{aligned}\nabla_\ell \mathcal{D}(\theta_c) &= \frac{\partial}{\partial \theta_{c,\ell}} \mathcal{D}(\theta_c) \\ &= \int_0^{\frac{2\pi}{\omega_0}} \frac{\partial}{\partial \theta_{c,\ell}} \left| \widetilde{i}_{\text{total}}(\tau, \theta_c) \right|^2 d\tau \\ &= \int_0^{\frac{2\pi}{\omega_0}} \underbrace{\frac{\partial}{\partial \widetilde{i}_\ell(\tau, \theta_{c,\ell})} |\widetilde{v}_x(\tau)|^2}_{\substack{\text{Compute from } v_x(t) \\ \text{measurement and (2)}}} + \frac{\partial}{\partial \theta_{c,\ell}} \underbrace{\widetilde{i}_\ell(\tau, \theta_{c,\ell})}_{\text{Compute from (2)}} d\tau.\end{aligned} \tag{6}$$

Importantly, it emerges that the gradient in (6) can be computed using variables that are locally sensed by the ℓth inverter, including its dc link voltage V_ℓ, a time domain measurement of the ac voltage $v_x(t)$ over an interval of length $2\pi/\omega_0$, and the filter inductance L_ℓ. Note that this inductance value (or other filter parameters) can be programmed into the inverter *a priori*. If this information is not available or is expected to vary substantially during operation due to parameter drift or operating-point-dependent variations, online parameter estimation techniques, such as those developed in [5], can be utilized.

The gradient update rule minimizes one component of the global optimization in (4) using only local information. Under the proposed scheme, each of the N inverters iteratively performs this component-wise update. By doing so, the overall system will reach a steady-state carrier phase spacing that is close to the globally optimal point, $\theta_c^\star$. A proof of convergence for a general n-dimensional nonconvex optimization problem is given in [24]. Moreover, although this method may converge to local minima of (4), numerical simulations and Monte Carlo analysis in [18] indicate that the distortion at a local minimum is similar to that of the global minimum, particularly as the size of the network increases.

B. Simulation Verification

We present a SPICE-based numerical simulation to verify the operation of the proposed decentralized carrier phase shifting algorithm. For the base case simulation scenario that follows, we consider the network from Fig. 1 with $N = 3$. The asymmetry is introduced with nonidentical dc-side voltages ($V_1 = 1.5$ p.u., $V_2 = 1.0$ p.u., $V_3 = 2.0$ p.u.) and nonidentical filter inductances ($L_1 = 0.5$ p.u., $L_2 = 1.0$ p.u., $L_3 = 2.0$ p.u.). Additional relevant simulation parameters are listed in Table I.

Fig. 7 illustrates the distortion $\mathcal{D}(\theta_c)$ plotted as a function of the carrier phase spacing θ_c in a two-dimensional plane (i.e., a two-dimensional projection of the surface plot in Fig. 2). We assume that the network is initialized at some θ_c^0. This phase spacing is arbitrary in that since there is no coordination between any of the inverters, their carrier phase spacing with respect to one another will be (initially) essentially random. The distortion at this initial point is 11.3 p.u. Moreover, we will assume, without loss of generality, that the inverters will perform their update step in a sequential ordering; we will show in Section V that this ordering can be arbitrary and does not impact the steady state convergence. At the first step, $\mathcal{I}_2$ will compute

TABLE I
PARAMETERS FOR SIMULATION AND EXPERIMENTAL PROTOTYPE

System Parameters	
v_{grid}	$230\ \text{V}_{\text{rms}}$, 60 Hz
L_ℓ	1 mH, 38 mΩ
ω_0	$2\pi\ \ 60\ \text{rad}\cdot\text{sec}^{-1}$
ω_c	$2\pi\ \ 20\times10^3\ \text{rad}\cdot\text{sec}^{-1}$
Z_{grid}	3 mH, 100 mΩ
Experimental Parameters	
v_{grid} Supply	Regatron ACS.50.528.72
L_ℓ	Hammond 157D
$V_1 \ldots V_3$ Supplies	Three Keysight RP7963A supplies
Control FPGA	Three Xilinx Artix-7 XC7A35T
v_x Sensor	LEM LV20-P voltage transducer

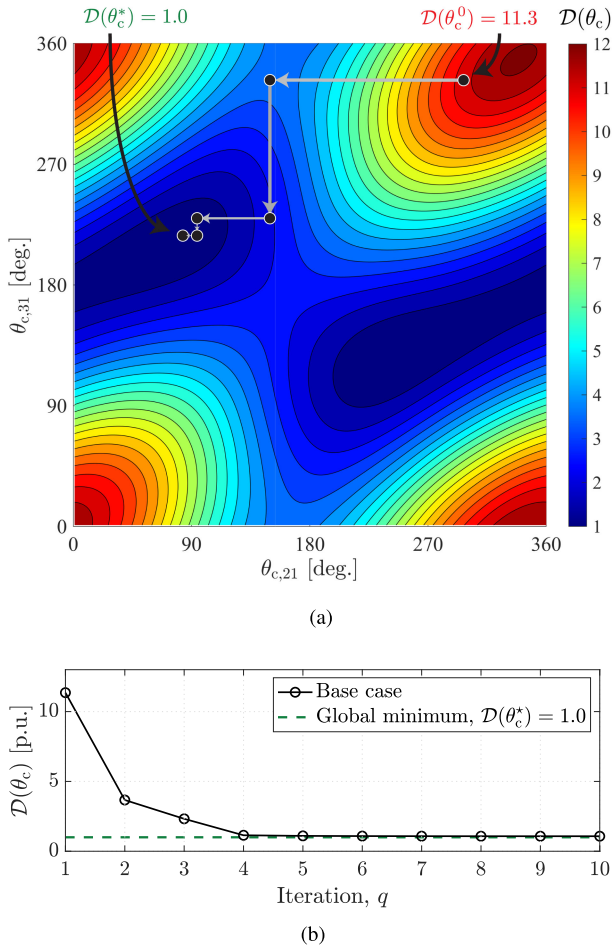


Fig. 7. SPICE-based numerical simulation of the proposed decentralized carrier phase shifting algorithm that seeks the optimal phase spacing $\theta_c^\star$ under ideal network scenarios (no line impedances). (a) A contour plot of $\mathcal{D}(\theta_c)$ for the simulated operating scenario along with an illustration of the component-wise optimization. (b) $\mathcal{D}(\theta_c)$ as a function of the component-wise iteration q. As shown, the global minimum $\mathcal{D}(\theta_c^\star)$ is effectively obtained by the fifth iteration of the optimization.

the carrier phase spacing that minimizes the $\theta_{c,21}$ component of $\mathcal{D}(\theta_c)$. This is illustrated in the first horizontal arrow that minimizes $\mathcal{D}(\theta_c)$ along the $\theta_{c,21}$ axis. At this point, $\mathcal{D}(\theta_c)$ has been reduced to 3.7 p.u. Subsequently, $\mathcal{I}_3$ will perform a similar operation in minimizing $\mathcal{D}(\theta_c)$ along the $\theta_{c,31}$ axis, as indicated with the vertical arrow. After approximately five such component-wise minimizations, the network has arrived

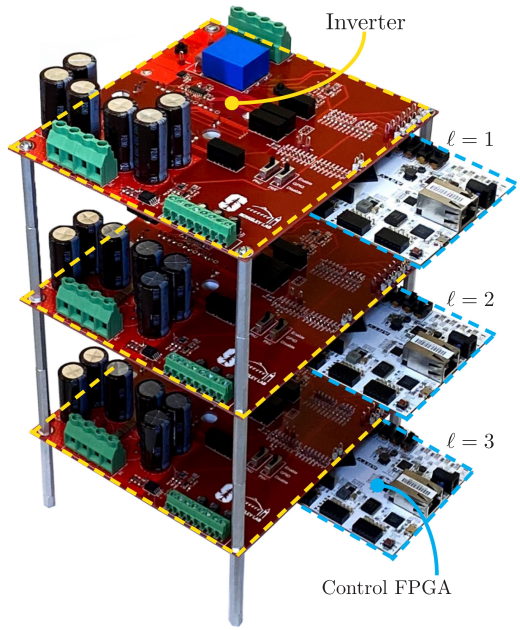


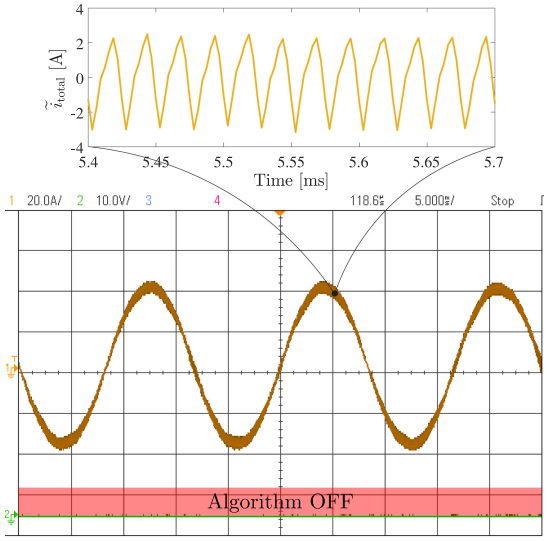
Fig. 8. Hardware prototype consisting of three 2-kW single-phase inverters.

at a carrier phase spacing that is effectively the optimal point $\theta_c^\star$, at which point $\mathcal{D}(\theta_c) = 1.0$ p.u. Fig. 7(b) illustrates this monotonic, approximately exponential reduction in distortion with each of the component-wise iterations q.

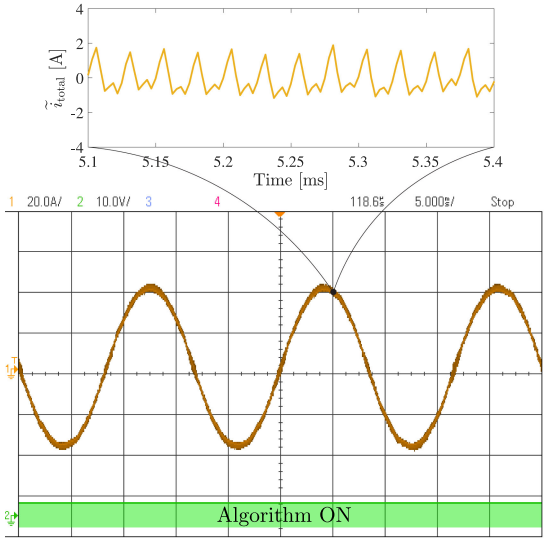
IV. EXPERIMENTAL RESULTS

In this section, we present experimental results to validate the analysis and algorithm presented in the preceding sections. A hardware prototype, shown in Fig. 8, consisting of three output-parallel connected single-phase inverters is used for the validation. Each inverter is rated to $30\ \text{V}_{\text{rms}}$ and can handle up to 2 kW. The dc ports in each inverter are connected to three separate Keysight RP7963A regenerative power supplies rated to 950 V to facilitate experiments with nonuniform input voltages. The ac ports of the inverters are connected in parallel to a Regatron ACS.50.528.72 50 kVA four-quadrant regenerative grid simulator and load. Each inverter is equipped with a Xilinx Artix-7 XC7A35T field-programmable gate array (FPGA) that hosts the inverter controller and the decentralized carrier phase shifting algorithm. Both the controller and the algorithm utilize 1424 slice LUT instances and 1171 slice register instances (6.84% and 2.82% of available board resources, respectively). The computational requirements for the algorithm are relatively low since the implementation utilizes basic arithmetic and integrator blocks. This is in contrast to other optimization methods (e.g., particle swarm optimization) that can require substantially higher resource allocation [18]. Each inverter also has the appropriate sensors and signal conditioning circuits for sampling v_x, V_ℓ, and i_ℓ. Table I lists values of pertinent parameters and components of the experimental setup.

We introduce asymmetry into this network by varying the dc link voltages of the individual inverters. In particular, we evaluate the operating point at which $V_1 = 1.5$ p.u., $V_2 = 1.0$ p.u., and $V_3 = 2.0$ p.u. ($V_1 = 488$ V, $V_2 = 325$ V, $V_3 = 651$ V). From



(a)



(b)

Fig. 9. Comparison of the total output current waveform i_{total} when the inverter carriers are (a) symmetrically interleaved and (b) optimally phase shifted with the proposed decentralized algorithm. (a) Symmetrically interleaved carrier phase shifting result in a peak-to-peak ripple in $\widetilde{i}_{\text{total}}$ of approximately 5.37 A. (b) When the carriers are optimally phase shifted using the decentralized carrier phase shifting algorithm, the peak-to-peak ripple in $\widetilde{i}_{\text{total}}$ is reduced to approximately 2.40 A.

Fig. 6(a), we predict a 2.6× reduction in $\mathcal{D}(\theta_{\text{c}})$ with this asymmetry when moving from the symmetric interleaved carrier phase spacing to the optimal phase spacing $\theta_{\text{c}}^{\star}$.

First, the steady state performance of the algorithm is verified. Fig. 9(a) illustrates the output current i_{total} when symmetric interleaved carrier phase spacing is applied to the three inverters. As shown in the magnified view, the peak-to-peak ripple in $\widetilde{i}_{\text{total}}$ is approximately 5.37A, resulting in a WTHD factor of 5.11%. When the decentralized carrier phase shifting algorithm is utilized, as shown in Fig. 9(b), the peak-to-peak ripple in $\widetilde{i}_{\text{total}}$ is 2.40A, resulting in a WTHD of 3.31%. This represents

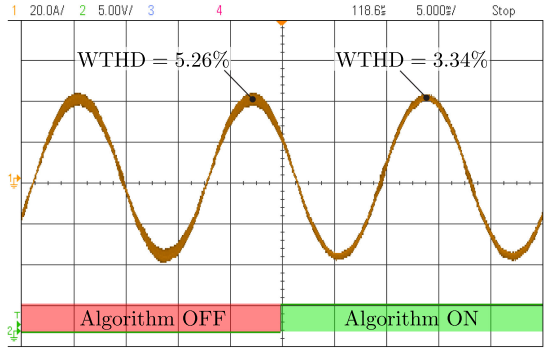


Fig. 10. The total output current waveform i_{total} before and after the proposed algorithm is initialized on each inverter at $t = 0$. As shown, the system is able to dynamically converge to the optimal carrier phase spacing that minimizes $\mathcal{D}(\theta_{\text{c}})$, and enables a 36.5% reduction in WTHD.

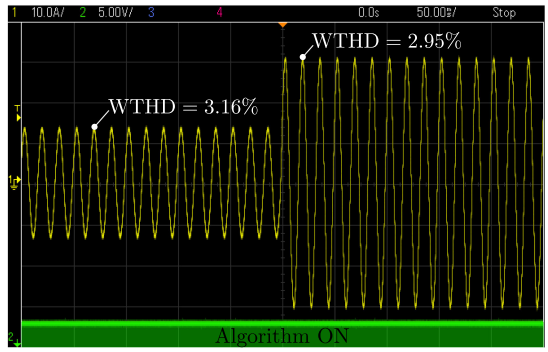


Fig. 11. The total output current, i_{total}, during a step transient when the total rms current increases by 10 A_{rms}. The carrier phase shifting algorithm continuously minimizes the ripple such that the WTHD is approximately the same before and after the transient.

a 36.3% reduction in WTHD, which corroborates the theoretical analysis.

Next, the transient performance of the algorithm is validated. As shown in Fig. 10, the inverter network is initialized without any coordination between the carriers of the individual inverters. This results in a WTHD of 5.26%. At $t = 0$, the decentralized algorithm is initialized on each individual inverter. In less than one line cycle (16.7ms), it can be seen that the ripple in the ac waveform has been dynamically minimized. The WTHD after the algorithm is initialized is 3.34%, a 36.5% reduction, which, again, confirms the analysis in Section II.

Finally, we evaluate the ability of the algorithm to minimize ripple during operating transients. In Fig. 11, the output current reference of $\mathcal{I}_3$ is initially 1 A_{rms}. In this operating state, the decentralized carrier phase shifting algorithm realizes a WTHD of 3.16%. At $t = 0$, the the output current reference of $\mathcal{I}_3$ is increased to 11 A_{rms}, and a corresponding 10 A_{rms} increase in i_{total} is observed. As shown, the algorithm adapts to this new operating point within one line cycle, and the WTHD remains approximately constant at 2.95%.

V. Analyzing Nonidealities and Other Practical Considerations

In this section, we consider the effects of nonidealities that emerge when implementing the proposed algorithm in typical

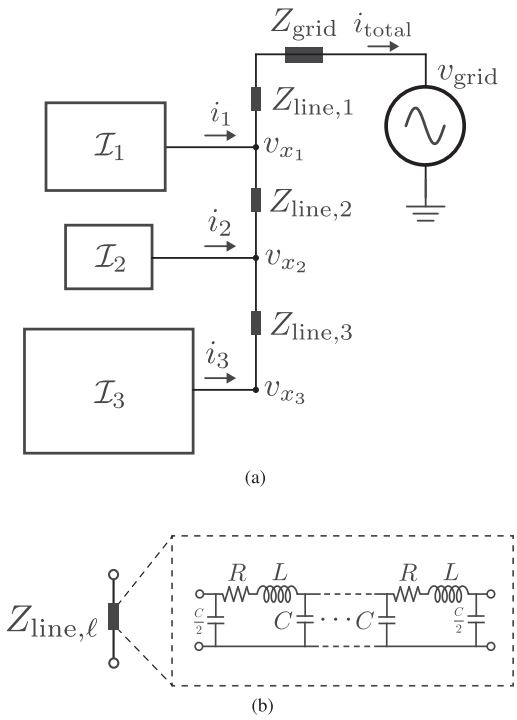


Fig. 12. The simulated network utilizes three single-phase inverters and incorporates a π-section line model to analyze the impact of nonnegligible distribution line dynamics. (a) The network topology model that incorporates distributed line dynamics between interconnected inverters. (b) The distribution line π-cell model is utilized to capture the dynamics of lines of various lengths and wire composition.

operating environments. In particular, we verify that the algorithm can suitably converge to the optimal carrier phase spacing even in the presence of nonnegligible line impedances that can be present in physically distributed inverter networks. Additionally, we discuss practical considerations of implementing the algorithm in real time, such as the selection of the iteration time step, and the resulting impact on the algorithm performance.

A. *Effects of Nonnegligible Line Impedances*

To analyze the impact of nonnegligible line impedances, we consider the network topology is illustrated in Fig. 12. As shown in Fig. 12(a), line impedances $Z_{\text{line},\ell}$ are included between the three adjacent inverters. The line is modeled as a cascaded π-cell model [see Fig. 12(b)] that can approximate the dynamics of lines of various lengths and wire composition [25].

In the base case scenario simulated in Section III-B, these line impedances were neglected, which implied that $v_x = v_{x_1} = v_{x_2} = v_{x_3}$. However, in the presence of these impedances, the sensed ac voltages of each inverter are no longer equivalent, that is, $v_{x_1} \neq v_{x_2} \neq v_{x_3}$. This is relevant since the optimization that each inverter performs utilizes a time domain measurement of this voltage, as indicated in (6).

Two line impedance models are tested that approximate a 5 m and 20 m length of distribution cable. These lengths are chosen to reflect the typical cable lengths in a single-phase distributed power generation system. The parameters of the π-cell models are listed in Table II. The results of the simulation for these

TABLE II
PARAMETERS FOR THE SIMULATED CABLE MODELS

Cable Parameters	Base Case	Model 1	Model 2
Length of cable modeled	0 m	5 m	20 m
Number of π-cells	-	4	16
L (per cell)	-	0.3 mH	0.3 mH
R (per cell)	-	12 mΩ	12 mΩ
C (per cell)	-	0.5 µF	0.5 µF

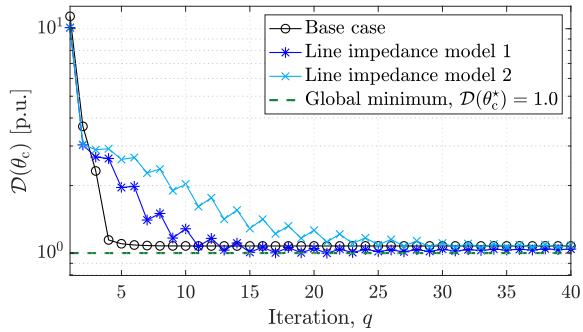


Fig. 13. SPICE-based numerical simulation for ideal and nonideal network scenarios. As shown, the presence of nonnegligible network impedances do not impact the ability of the decentralized algorithm in obtaining the global minimum $\mathcal{D}(\theta_c^\star)$. However, larger network impedances increase the number of iterations required for convergence.

models are shown in Fig. 13 and are compared with the ideal network. As shown, the presence of the line impedances do not significantly impact the ability of the decentralized algorithm in obtaining the global minimum $\mathcal{D}(\theta_c^\star)$, as all three scenarios are able to converge to this point. However, the larger line impedances increase the number of iterations required for convergence. The 5 m line model requires approximately fifteen iterations to reach $\mathcal{D}(\theta_c^\star)$, while the 20 m line model requires approximately thirty iterations. In comparison, the base case network that neglects the line impedances requires about five iterations.

B. *Iteration Time Step and Implementation Considerations*

The iteration time step, that is, the algorithm update rate for each individual inverter, is a design variable that influences certain aspects of the algorithm performance. In practice, and in the experiment results, this update rate is selected to be ten times slower than the switching frequency (that is, $\omega_c/10$). This slower loop allows the relevant carrier frequency dynamics to reach a steady state from the perturbation of the updated carrier phase shift. For a carrier frequency of 20 kHz, each inverter would update its carrier phase shift every 500 μs. Thus, for the above simulations, the ideal network would converge in 2.5 ms (five iterations) while the 20 m line impedance model would converge in 15 ms (thirty iterations). Both scenarios would converge within one line frequency cycle (16.7 ms).

Additionally, two assumptions are made that reconcile the analytical derivation in Section III with practical considerations and the need for complete decentralization. First, we make the assumption that any two inverters will not be executing the algorithm simultaneously. This is a reasonable assumption since the computation time for each algorithm update is small in

comparison to the update rate. For example, the implementation on the Xilinx Artix-7 XC7A35T requires 5 μs to compute the updated optimal phase shift. This is one hundred times faster than the algorithm update rate; thus it is unlikely that any two inverters would make the computation simultaneously.

Second, while the analysis and simulation above assumed that the algorithm iterates on each inverter $\mathcal{I}_\ell$ in a sequential manner from $\mathcal{I}_1$ to $\mathcal{I}_N$, we note that, both mathematically and in practice, the ordering does not affect the convergence to the minimum. Fig. 7(a) provides intuition that component-wise minimization in any ordering will drive the system to some local minima of $\mathcal{D}(\theta_c)$. Importantly, the magnitude of $\mathcal{D}(\theta_c)$ at either of the two local minima in figure are approximately identical. Moreover, the general n-dimensional proof of the algorithm (see [24]) makes no assumptions on component-wise ordering. The validity of both of these assumptions (as was demonstrated in Section IV) is relevant in practice since it eliminates the need for precise timing or synchronization between inverters.

VI. Conclusion and Future Work

This article has analyzed and experimentally validated a technique for minimizing distortion and improving power quality for networks of inverters with decentralized carrier phase shifting. In particular, the work considers asymmetric parallel-connected single-phase inverters whereby asymmetries arise from either nonuniform operating conditions or from variations in passive components. We have demonstrated that for certain asymmetries, the optimal carrier phase shifting can enable an order-of-magnitude improvement ($18.3\times$) compared to the worst-case carrier phase shifting, and also universal improvements compared to symmetric carrier interleaving. Importantly, our proposed algorithm for dynamically tracking this optimal carrier phase shifting is completely decentralized, requiring no communication or information exchange between inverters. This is unique compared to existing literature and has important practical benefits for implementation, including improved robustness and reduced cost. The proposed design and analysis techniques can be applied to larger and more general networks of inverters, for instance, three-phase inverters or inverters that are connected in series or parallel at the input or output. Additionally, other optimization algorithms can be explored to compute optimal carrier phase spacing for minimizing distortion, such as those based on the gradient method or a metaheuristic optimizer.

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